Department of Telecommunications Engineering

NED University of Engineering &Technology

LABORATORY WORKBOOK

DIGITAL LOGIC DESIGN
(TC-201)

Instructor Name: _____

Student Name: _____

Roll Number: _____ **Batch:** _____

Semester: _____ **Year:** _____

Department: _____

LABORATORY WORKBOOK

For the Course

DIGITAL LOGIC DESIGN

(TC-203)

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Approved By:
The Board of Studies of Department of Telecomunications Engineering

INTRODUCTION

Digital Logic Design Practical Workbook covers those practicals that are very knowledgeable and quite beneficial in grasping the core objective of the subject. These practicals solidify the theoretical and practical concepts that are very essential for the engineering students.

This work book comprise of practicals covering the topics of Digital Logic Design that are arranged on modern concepts. Above all this workbook contains a relevant theory about the Lab session.

CONTENTS

LAB SESSION 01

OBJECTIVE:

To analyze the functionality of basic logic gates.

THEORY:

A logic gate is an elementary building block of a digital circuit. Most logic gates have two inputs and one output. At any given moment, every terminal is in one of the two binaryconditions *low* (0) or *high* (1), represented by different voltage levels. The logic state of a terminal can, and generally does, change often, as the circuit processes data. In most logic gates, the low state is approximately zero volts (0 V), while the high state is approximately five volts positive (+5 V).

There are seven basic logic gates: AND, OR, XOR, NOT, NAND, NOR, and XNOR.

AND GATE:

The *AND gate* is so named because, if 0 is called "false" and 1 is called "true," the gate acts in the same way as the logical "and" operator. The following illustration and table show the circuit symbol and logic combinations for an AND gate. (In the symbol, the input terminals are at left and the output terminal is at right.) The output is "true" when both inputs are "true."Otherwise, the output is "false."

AND gate

Input 1	Input 2	Output
0	0	0
0	1	0
1	0	0
1	1	1

OR GATE:

The *OR gate* gets its name from the fact that it behaves after the fashion of the logical inclusive "or." The output is "true" if either or both of the inputs are "true." If both inputs are "false," then the output is "false."

OR gate

Input 1	Input 2	Output
0	0	0
0	1	1
1	0	1
1	1	1

XOR GATE:

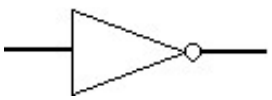
The *XOR* (*exclusive-OR*) *gate* acts in the same way as the logical "either/or." The output is "true" if either, but not both, of the inputs are "true." The output is "false" if both inputs are "false" or if both inputs are "true." Another way of looking at this circuit is to observe that the output is 1 if the inputs are different, but 0 if the inputs are the same.

XOR gate

Input 1	Input 2	Output
0	0	0
0	1	1
1	0	1
1	1	0

NOT GATE:

A logical *inverter*, sometimes called a *NOT gate* to differentiate it from other types of electronic inverter devices, has only one input. It reverses the logic state.



Inverter or NOT gate

Input	Output
1	0
0	1

NAND GATE:

The *NAND gate* operates as an AND gate followed by a NOT gate. It acts in the manner of the logical operation "and" followed by negation. The output is "false" if both inputs are "true." Otherwise, the output is "true."

NAND gate

Input 1	Input 2	Output
0	0	1
0	1	1
1	0	1
1	1	0

NOR GATE:

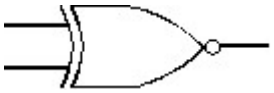
The *NOR gate* is a combination OR gate followed by an inverter. Its output is "true" if both inputs are "false." Otherwise, the output is "false."

NOR gate

Input 1	Input 2	Output
0	0	1
0	1	0
1	0	0
1	1	0

XNOR GATE:

The *XNOR (exclusive-NOR) gate* is a combination XOR gate followed by an inverter. Its output is "true" if the inputs are the sameand"false" if the inputs are different.



XNOR gate

Input 1	Input 2	Output
0	0	1
0	1	0
1	0	0
1	1	1

Using combinations of logic gates, complex operations can be performed. In theory, there is no limit to the number of gates that can be arrayed together in a single device. But in practice, there is a limit to the number of gates that can be packed into a given physical space. Arrays of logic gates are found in digital integrated circuits (ICs). As IC technology advances, the required physical volume for each individual logic gate decreases and digital devices of the same or smaller size become capable of performing ever-more-complicated operations at ever-increasing speeds.

Common Gate ICs:

Part number	Description
7400	Quad 2-Input NAND gate
7402	Quad 2-Input NOR gate
7408	Quad 2-Input AND gate
7410	Triple 3-Input NAND gate
7432	Quad 2-Input OR gate
7486	Quad 2-Input XOR gate

LABORATORY TASK:

1) Power up the 2-input AND , OR and NOT TTL ICs on a bread board.
2) Apply inputs using push-to-on/off switches and observe the output via LEDs.
3) Fill the Table provided in the result area.

RESULT:

A	B	A.B	A+B	A'
0	0			
0	1			
1	0			
1	1			

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LAB SESSION 02

OBJECTIVE:

Design and Implement Combinational circuits using discrete logic gates.

PRE-LAB TASKS:

- Review the class lecture regarding the design of a combinational Circuit.
- Read section 2.6 of the reference book [1].
- Complete Lab Session 01 of the manual.
- Read the functionality of Half Adder, Full Adder, and parity encoder from the internet.

EQUIPMENT REQUIRED:

- AND, OR, Inverter gates ICs (IC Numbers are given in lab 1)
- LEDs
- Bread Boards
- Power Supply / 9 Volt battery and a voltage regulator IC (7805)
- Multimeter

TASKS:

Task 1: Design and Implement Half Adder

A. Draw the truth table of Half adder.
B. Design the circuit of the Half adder using the product of sum (PoS).
C. Implement the circuit using Inverter, AND, and OR logic gates.

Task 2: Design and Implement Full Adder

A. Draw the truth table of Full adder.
B. Design the circuit of the Full adder using the sum of the product (SoP).
C. Implement the circuit using Inverter, AND, and OR logic gates.

Task 3: Design a circuit for parity encoder that outputs 5 bits odd parity codes for the 4 bits input.

A. Draw the truth table.

B. Design the circuit using the product of sum (PoS).

C. Implement the circuit using Inverter, AND, and OR logic gates.

Reference Book:

[1] Brown, Stephen. "Fundamentals of digital logic design with VHDL.", 3rd ed, 2010.

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LAB SESSION 03

OBJECTIVE:

Design and implement a multi-bit adder and subtractor using logic gates ICs.

PRE-LAB TASKS:

- Review the class lecture regarding the design of multi-bit adder and subtractor.
- Read section 5.2.1, 5.3.1, 5.3.2, and 5.3.3 of reference book [1].
- Complete Lab Session 02 of the manual.

EQUIPMENT REQUIRED:

- Logic gates ICs (IC Numbers are given in lab 1)
- LEDs
- Bread Boards
- Power Supply / 9 Volt battery and a voltage regulator IC (7805)
- Multimeter
- Switches.

TASKS:

Task1: Design and implement a 4-bit adder.

A. Design the 4-bit adder using a full adder and half adder design in Lab Session 01.

B. Implement the 4-bit adder circuit using logic gates IC.

C. Verify the functionality of physicaly implemented circuit.

Task2: Design and implement 4-bit subtractor

A. Design the 4-bit subtractor using the 4-bit adder designed in Task 1 of the current lab session.

B. Implement the 4-bit subtractor using logic gates IC.

C. Verify the functionality of physicaly implemented circuit.

Reference Book:

[1] Brown, Stephen. "Fundamentals of digital logic design with VHDL.", 3rd ed, 2010.

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LAB SESSION 04

OBJECTIVE:

To analyze the operation of BCD to 7-segment decoder.

PRE-LAB TASKS:

- Understand the operation of seven segment display.
- Download and understand the data sheet of IC 4511.

THEORY:

Binary Coded Decimal (BCD) is a way to express each decimal digit (0-9) with a binary code of four bits (0000-1001). With 4 bits, sixteen numbers (0000-1111) can be represented but in BCD only ten of these are used. The six codes combinations that are not used are called “invalid codes”.

A BCD to 7-segment display decoder such as 4511, has 4 BCD inputs and 7 output lines, one for each LED segment. The 4511 is designed to drive a common cathode display and won't work with a common anode display. In a common cathode display, the cathodes of all the LEDs are joined together and the individual segments are illuminated by HIGH voltages. If invalid codes, binary values greater than 1001, are connected to the inputs of the 4511, the outputs are all 0's and the display is blank.

Tasks:

Task1: Display the BCD code equivalent decimal digital on seven segment display.

A. Implement the circuit using BCD decoder IC 4511 and common cathode seven-segment display.

B. Verify the operation of the physical circuit and fill in the table given in the observation section.

OBSERVATIONS:

BCD Inputs				Segment Outputs							Display
D	C	B	A	a	b	c	d	e	f	g	
0	0	0	0								
0	0	0	1								
0	0	1	0								
0	0	1	1								
0	1	0	0								
0	1	0	1								
0	1	1	0								
0	1	1	1								
1	0	0	0								
1	0	0	1								
1	1	1	1								

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LAB SESSION 05

OBJECTIVE:

To design and implement combinational circuits using multiplexer and demultiplexer.

EQUIPMENTS:

- IC type 7404 HEX inverter
- IC type 7408 quad 2-input AND gate
- IC type 74151 8x1 multiplexer (1)
- IC type 74153 dual 4x1 multiplexer (2)
- IC type 7446 BCD-to-Seven-Segment decoder (1)
- Resistance network (1)
- Seven-Segment Display (1)

THEORY:

74151 is a 8 line-to-1 line multiplexer. It has the schematic representation shown in Fig 1. Selection lines S2, S1 and S0 select the particular input to be multiplexed and applied to the output.
Strobe S acts as an enable signal. If strobe =1, the chip 74151 is disabled and output y = 0. If strobe = 0 then the chip 74151 is enabled and functions as a Multiplexer. Table 1 shows the multiplex function of 74151 in terms of select lines.

Table 1.

Strobe	Select Lines			Output
S	S_2	S_1	S_0	Y
1	X	X	X	0
0	0	0	0	D0
0	0	0	1	D1
0	0	1	0	D2
0	0	1	1	D3
0	1	0	0	D4
0	1	0	1	D5
0	1	1	0	D6
0	1	1	1	D7

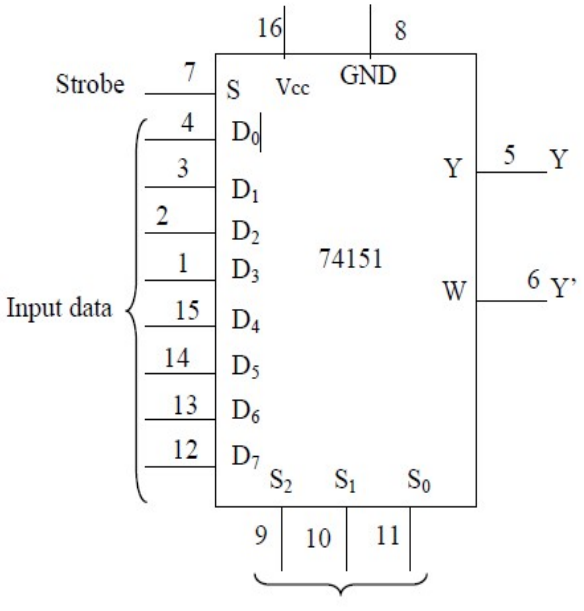

Fig.1 IC type 74151 Multiplexer 8×1

74153 is a dual 4 line-to-1 line multiplexer. It has the schematic representation shown in Fig 2. Selection lines S1 and S0 select the particular input to be multiplexed and applied to the output IY{1 = 1, 2}.Each of the strobe signals *IG* {I = 1, 2} acts as an enable signal for the corresponding multiplexer.

Table 2.shows the multiplex function of 74153 in terms of select lines. Note that each of the on-chip multiplexers act independently from the other, while sharing the same select lines S1 and S0.

Table 2

	Multiplexer 1		
Strobe	Select lines		Output
1G	S_1	S_0	1Y
1	X	X	0
0	0	0	$1D_0$
0	0	1	$1D_1$
0	1	0	$1D_2$
0	1	1	$1D_3$

	Multiplexer 2		
Strobe	Select lines		Output
2G	S_1	S_0	2Y
1	X	X	0
0	0	0	$2D_0$
0	0	1	$2D_1$
0	1	0	$2D_2$
0	1	1	$2D_3$

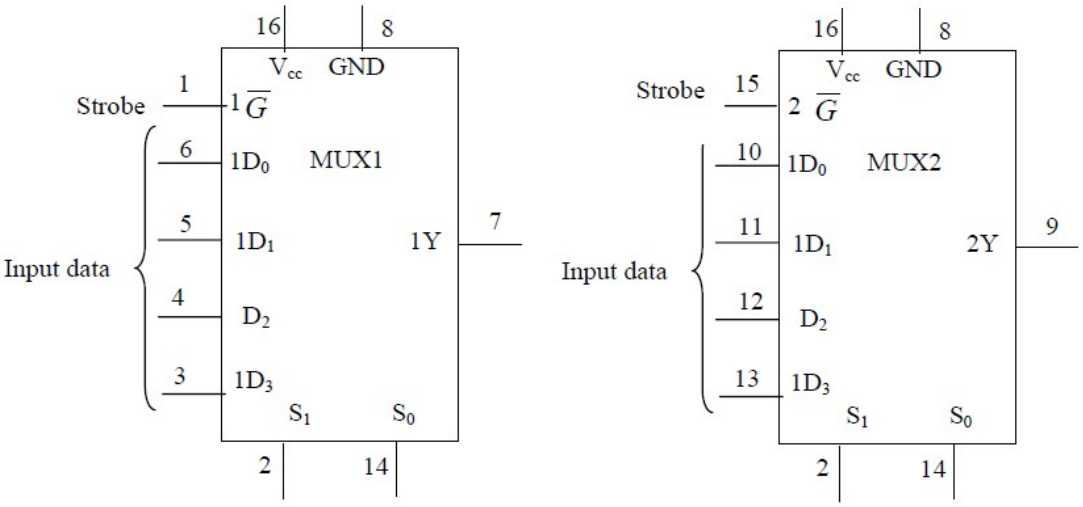

Fig.2 Pinout of 74153

IC 7446 is a BCD to seven segment decoder driver. It is used to convert the Combinational circuit outputs in BCD forms into 7 segment digits for the 7 segment LED display units.

PROCEDURE:

Part I: Parity Generator:

a) Design a parity generator by using a 74151 multiplexer. Parity is an extra bit attached to a code to check that the code has been received correctly.Odd parity bit means that the number of 1's in the code including the parity bit is an odd number. Fill the output column of the truth table in Table 2 for a 5-bit code in which four of the bits (A,B,C,D) represents the information to be sent and fifth bit (x), represents the parity bit. The required parity is an odd parity.
The inputs B,C and D correspond to the select inputs of 74151. Complete the truth table in Table 3 by filling in the last column with 0,1,A or A'.

b) Implement the circuit on breadboard , use 74-151 multiplexer and Binary switches for inputs and Binary Probes for outputs. The 74151 has one output for Y and another inverted output W. Use A and A' for providing values for inputs 0-7. The internal values "A, B, C" are used for selection inputs B,C, and D. Simulate the circuit and test each input combination filling in the table shown below. In the Lab connect the circuit and verify the operations. Connect an LED to the multiplexer output so that it represents the parity bit which lights any time when the four bits input have even parity.

Inputs				Outputs	Connect data to
A	B	C	D	X	
0	0	0	0		
0	0	0	1		
0	0	1	0		
0	0	1	1		
0	1	0	0		
0	1	0	1		
0	1	1	0		
0	1	1	1		
1	0	0	0		
1	0	0	1		
1	0	1	0		
1	0	1	1		
1	1	0	0		
1	1	0	1		
1	1	1	0		
1	1	1	1		

Table 2

Part 2: Vote Counter:

A committee is composed of a chairman (C), a senior member (S), and a member (M).
The rules of the committee state that:

- The vote of the member (M) will be counted as 2 votes
- The vote of the senior member will be counted as 3 votes.
- The vote of the chairman will be counted as 5 votes.

Each of these persons has a switch to close (“l”) when voting yes and to open (“0”) when voting no.

It is necessary to design a circuit that displays the total number of votes for each issue. Use a seven segment display and a decoder to display the required number. If all members vote no for an issue the display should be blank. (Recall from Experiment #5, that a binary input 15 into the 7446 blanks all seven segments).

If all members vote yes for an issue, the display should be 0. Otherwise the display shows a decimal number equal to the number of 'yes' votes. Use two 74153 units, which include four multiplexers to design the combinational circuit that converts the inputs from the members’ switch to the BCD digit for the 7446.

Use +5V for Logic 1 and ground for Logic 0 and use switches for C, S,and M. Use two chips 74153 and one decoder 7446 verify your design and get a copy of your circuit with the pin numbers to Lab so that you could connect the hardware in exactly the same way.

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Equipment Handling*Equipment care* during the use.	Doesn't handle equipment with required care.	Rarely handles equipment with required care.	Occasionally handles equipment with required care.	Often handles equipment with required care.	Handles equipment with required care.
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Laboratory Session No. _____ Date: _____

Weighted CLO (Psychomotor Score)	
Remarks	
Instructor's Signature with Date:	

LAB SESSION 06

OBJECTIVE:

- Able to write synthesizable code of combinational circuits using concurrent assignment and primitives.
- Able to simulate the Verilog code on ModelSim or QuestaSim (Intel Edition).
- Able to synthesize the code and burn it in FPGA using Intel Quartus Prime.

PRE-LAB TASKS:

- Review the class lecture regarding Verilog coding for combinational circuits.
- Review the lecture regarding Quartus and Model Sim.
- Read sections 4.1 and 4.2 of the reference book [1].
- Download the DE1-SoC manual and understand the pin configuration of switches and LEDs.
- Complete Lab Session 03 of the manual.

Equipment/Software Required:

- Intel Quartus Prime (Lite Edition)
- Questa or ModelSim (Intel Edition)
- FPGA Board (DE-1SoC Board)

TASKS:

Task 1 Implement the Half Adder circuit design in Lab Session 01 on FPGA.

A. Write the synthesizable Verilog code of Half Adder using primitives.

B. Simulate the verilog code on ModelSim (Intel Edition) and functionally verify your design.

C. Synthesize the verilog code and burn it on FPGA.

D. Physically verify the functionality of the design on FPGA.

Task 2: Implement the Full Adder circuit design in Lab Session 01 on FPGA.

A. Write the synthesizable Verilog code of Full Adder using Concurrent Assignment.
B. Simulate the verilog code on ModelSim (Intel Edition) and functionally verify your design.
C. Synthesized the verilog code and burn it on FPGA.
D. Physically verify design on FPGA.

Task 3: Implement the parity encoder circuit design in Lab Session 01 on FPGA.

A. Write the synthesizable Verilog code of parity encoder using either Concurrent Assignment or primitives.
B. Simulate the verilog code on ModelSim (Intel Edition) and functionally verify your design.
C. Synthesize the verilog code and burn it on FPGA.
D. Physically verify design on FPGA.

Reference Book:

[1] Harris, Sarah L., and David Harris. Digital Design and Computer Architecture, RISC-V Edition. Morgan Kaufmann, 2021.

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Department of _____ Engineering
Course Code and Title: _____

Psychomotor Domain Assessment Rubric-Level P3					
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Equipment Use Sensory skills to ***demonstrate*** the use of the equipment for the lab work.	Doesn't demonstrate the use of equipment.	Slightly demonstrates the use of equipment.	Somewhat demonstrates the use of equipment.	Moderately demon strates the use of equipment.	Fully demonstrates the use of equipment.
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Laboratory Session No. _____ Date: _____

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Remarks	
Instructor's Signature with Date:	

LAB SESSION 07

OBJECTIVE:

- Implement Multi-bit Adder on FPGA.
- Implement Multi-bit Subtractor on FPGA.

PRE-LAB TASKS:

- Review the class lecture regarding Verilog coding for combinational circuits.
- Review the lecture regarding Quartus and Model Sim.
- Read sections 4.3 of the reference book [1].
- Download the DE1-SoC manual and understand the pin configuration of switches and LEDs.
- Complete Lab Session 04 of the manual.
- Complete Lab Session 06 of the manual.

Equipment/Software Required:

- Intel Quartus Prime (Lite Edition)
- Questa or ModelSim (Intel Edition)
- FPGA Board (DE-1SoC Board)

TASKS:

Task1: Implement the 4-bit Adder circuit design in Lab Session 04 on FPGA.

A. Write the synthesizable Verilog code 4-bit Adder using the half adder and full adder module written in Lab Session 06.

B. Simulate the verilog code on ModelSim (Intel Edition) and functionally verify your design.

C. Synthesize the verilog code and burn it on FPGA.

D. Physically verify design on FPGA.

Task2: Implement the 8 bit Adder circuit design on FPGA.

A. Write the synthesizable Verilog code 8-bit Adder using the 4-bit Adder module design in Task1 of the current Lab Session.

B. Simulate the verilog code on ModelSim (Intel Edition) and functionally verify your design.

C. Synthesize the verilog code and burn it on FPGA.

D. Physically verify design on FPGA.

Task3: Implement the 8 bit Subtractor circuit design on FPGA.

A. Write the synthesizable Verilog code 8-bit Subtractor using the 8-bit Adder module design in Task2 of the current Lab Session.

B. Simulate the verilog code on ModelSim (Intel Edition) and functionally verify your design.

C. Synthesize the verilog code and burn it on FPGA.

D. Physically verify design on FPGA.

Reference Book:

[1] Harris, Sarah L., and David Harris. Digital Design and Computer Architecture, RISC-V Edition. Morgan Kaufmann, 2021.

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Laboratory Session No. _____ Date: _____

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Remarks	
Instructor's Signature with Date:	

LAB SESSION 08

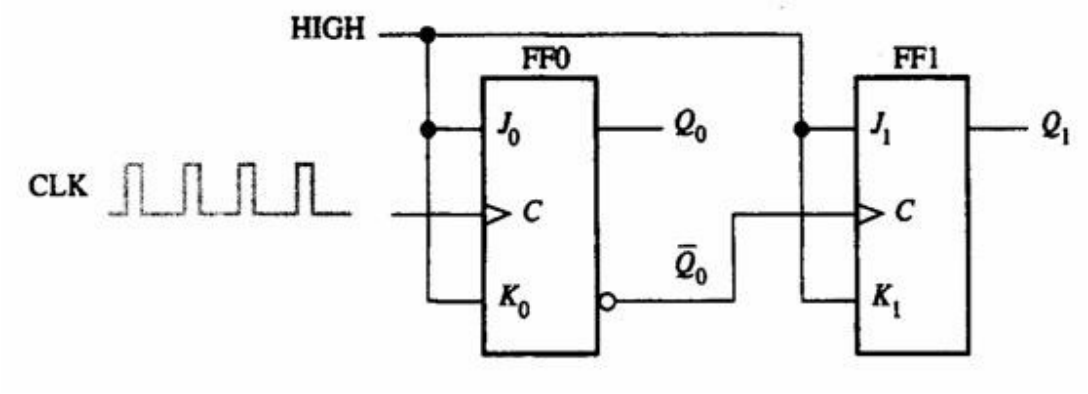
OBJECTIVE:

To design and implement a two bit asynchronous and synchronous binary counters using J K flip flops.

THEORY:

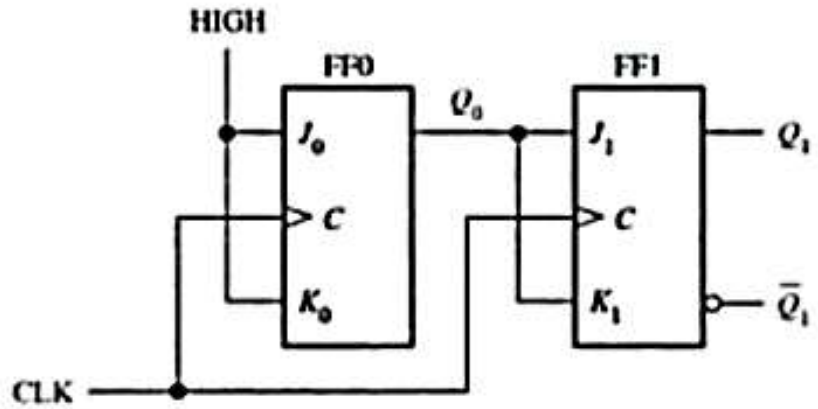
2 BIT ASYNCHRONOUS COUNTER:

Asynchronous counter is one in which flip flops within the counter do not change states at exactly the same time because they do not have a common clock pulse.



2 BIT SYNCHRONOUS COUNTER:

Synchronous counter is one in which all the flip flops are clocked at the same time by a common clock pulse.



OBSERVATIONS:

Clk	Q1	Qo
1↑		
2↑		
3↑		
4↑		

RESULT:

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Department of _____ Engineering
Course Code and Title: _____

Psychomotor Domain Assessment Rubric-Level P3					
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EquipmentIdentification Sensory skill to ***identify*** equipment and/or its component for a lab work.	Not able to identify the equipment.	--	--	--	Able to identify equipment as well as itscomponents.
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Remarks	
Instructor's Signature with Date:	

LAB SESSION 9

OBJECTIVE:

To analyze and study the operations of the following circuits:

- RS and Clocked RS Latch
- D Latch

THEORY:

So far you have encountered with *combinatorial logic*, i.e. circuits for which the output depends only on the inputs. In many instances it is desirable to have the next output depending on the current output. A simple example is a *counter*, where the next number to be output is determined by the current number stored. Circuits that remember their current output or state are often called *sequential logic* circuits. Clearly, sequential logic requires the ability to store the current state. In other words, *memory* is required by sequential logic circuits, which can be created with Boolean gates. If you arrange the gates correctly, they will remember an input value. This simple concept is the basis of RAM (random access memory) in computers, and also makes it possible to create a wide variety of other useful circuits.

Memory relies on a concept called **feedback**. That is, the output of a gate is fed back into the input. The simplest possible feedback circuit using two inverters is shown below (Fig.1):

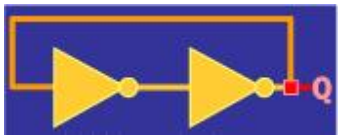


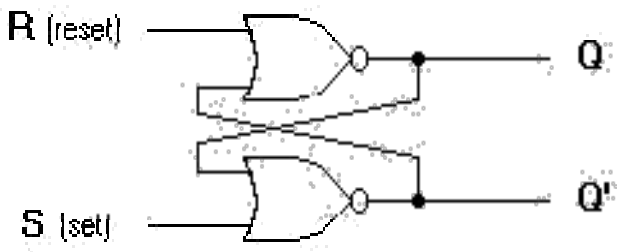
Fig.1: Simplest realization of feedback circuit

If you follow the feedback path, you can see that if Q happens to be 1 (or 0), it will always be 1 (or 0). Since it's nice to be able to control the circuits we create, this one doesn't have much use -- but it does let you see how feedback works. It turns out that in "real" sequential circuits, you can actually use this sort of simple inverter feedback approach. The memory elements in these circuits are called *Latch*. A Latch circuit has two outputs, one for the normal value and one for the complement value of the stored bit. Binary information can enter a Latch in a variety of ways and gives rise to different types of Latch.

RS Latch

RS Latch is the simplest possible memory element. It can be constructed from two NAND gates or two NOR gates. Let us understand the operation of the RS Latch using NOR gates as shown below using the truth table for 'A NOR B' gate. The inputs R and S are referred to as the Reset and Set inputs, respectively. The outputs Q and Q' are complements of each other and are referred to as the normal and complement outputs, respectively. The binary state of the latch is taken to be the value of the normal output. When Q=1 and Q'=0, it is in the *set state* (or 1-state). When Q=0 and Q'=1, it is in the *reset/clear state* (or 0-state).

Circuit Diagram:



A	B	$\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

S=1 and R=0: The output of the bottom NOR gate is equal to zero, Q'=0. Henceboth inputs to the top NOR gate are equal to 0, thus, Q=1. Hence, the input combination S=1 and R=0 leads to the latch being **set** to Q=1.
S=0 and R=1: Similar to the arguments above, the outputs become Q=0 andQ'=1. We say that the latch is **reset**.
S=0 and R=0: Assume the latch was previously in set (S=1 and R=0)condition. Now changing S to 0 results Q' still at 0 and Q=1. Similarly, when the latch was previously in a reset state (S=0 and R=1), the outputs do not change. Therefore, with inputs S=0 and R=0, the latch holds its state.
S=1 and R=1: This condition violates the fact that both outputs are complementsof each other since each of them tries to go to 0, which is not a stable configuration. It is impossible to predict which output will go to 1 and which will stay at 0. In normal operation this condition must be avoided by making sure that 1's are not applied to both inputs simultaneously, thus making it one of the main disadvantages of RS latch.

All the above conditions are summarized in the characteristic table below:

Characteristic Table:

R	S	Q	Q’	Comment
0	0	Q	Q’	Hold state
0	1	1	0	Set
1	0	0	1	Reset
1	1	?	?	Indeterminate

Debounce circuit

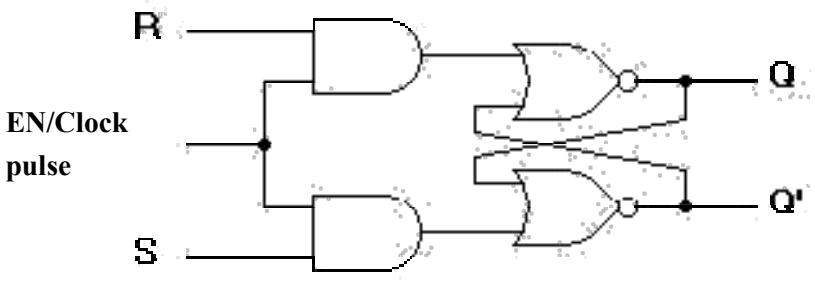
An elementary example using this latch is the debounce circuit. Suppose a piece of electronics is to change state under the action of a mechanical switch. When this switch is moved from position S to R (S=0, R=1), the contacts make and break several times at R before settling to good contact. It is desirable that the electronics should respond to the first contact and then remain stable, rather than switching back and forth as the circuit makes and breaks. This is achieved by RS flip-flop which is reset to Q=0 by the first signal R=1 and remains in a fixed state until the switch is moved back to position S, when the signal S=1 sets the flip-flop to Q=1.

Gated or Clocked RS Latch

It is sometimes desirable in sequential logic circuits to have a bistable RS Latach that only changes state when certain conditions are met regardless of the condition of either the Set or the Reset inputs. By connecting a 2-input AND gate in series with each input terminal of the RS NOR latch a Gated RS latch can be created. This extra conditional input is called an "Enable" input and is given the prefix of "EN" as shown below. When the Enable input "EN" = 0, the outputs of the two AND gates are also at logic level 0, (AND Gate principles) regardless of the condition of the two inputs S and R, latching the two outputs Q and Q’ into their last known state. When the enable input "EN" = 1, the circuit responds as a normal RS bistable latch with the two AND gates becoming transparent to the Set and Reset signals. This Enable input can also be connected to a clock timing signal adding clock synchronisation to the flip-flop creating what is sometimes called a "Clocked SR latch ".

So a **Gated/Clocked RS Latch** operates as a standard bistable latch but the outputs are only activated when a logic "1" is applied to its EN input and deactivated by a logic "0". The property of this flip-flop is summarized in its characteristic table where Qn
is the logic state of the previous output and Qn+1 is that of the next output and the clock input being at logic 1 for all the R and S input combinations.

Circuit Diagram:



Characteristic Table:

Qn	R	S	Qn+1
0	0	0	0 (Hold)
0	1	0	0
0	0	1	1
0	1	1	Indeterminate
1	0	0	1 (Hold)
1	1	0	0
1	0	1	1
1	1	1	Indeterminate

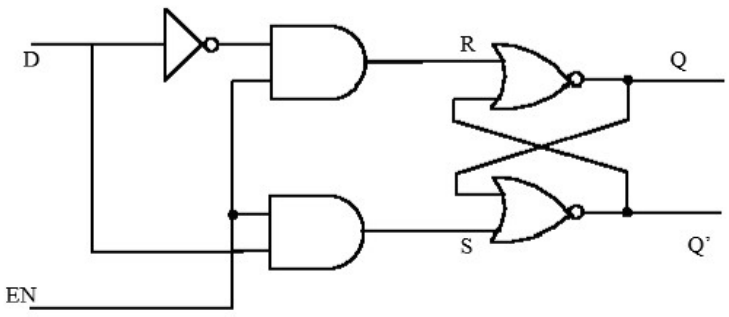
D Latach

An RS Latch is rarely used in actual sequential logic because of its undefined outputs for inputs R= S= 1. It can be modified to form a more useful circuit called D Latach, where D stands for data. The D flip-flop has only a single data input D as shown in the circuit diagram. That data input is connected to the S input of an RS flip-flop, while the inverse of D is connected to the R input. To allow the flip-flop to be in a holding state, a D- latch has a second input called Enable, EN. The Enable-input is AND-ed with the D-input.

When **EN=0**, irrespective of D-input, the R = S = 0 and the **state is held**.
When **EN= 1**, the S input of the RS flip-flop equals the D input and R is the inverse of D. Hence, output **Q follows D**, when EN= 1. When **EN returns to 0**, the most recent input **D is 'remembered'**.

The circuit operation is summarized in the characteristic table for **EN=1**.

Circuit Diagram:



Characteristic Table:

Qn	D	Qn+1
0	0	0
0	1	1
1	0	0
1	1	1

PROCEDURE:

1. Assemble the circuits one after another on your breadboard as per the circuit diagrams. Circuit diagrams given here do not show connections to power supply and LEDs assuming that you are already familiar with it from your previous lab experience.
2. Connect the ICs properly to power supply (pin 14) and ground (pin 7) following the schematics for ICs given above.
3. Using dip switch and resistors, facilitate all possible combinations of inputs from the power supply. Use the switch also to facilitate pulse input to the circuit.
4. Turn on power to your experimental circuit.
5. For each input combination, note the logic state of the normal and complementary outputs as indicated by the LEDs (ON = 1; OFF = 0), and record the results in a table.
6. Compare your results with the characteristic tables.
7. When you are done, turn off the power to your experimental circuit.

OBSERVATIONS:

Table for RS latch:

Table for Gated RS latch:

Table for D latch:

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Department of _____ Engineering
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Laboratory Session No. _____ Date: _____

Weighted CLO (Psychomotor Score)	
Remarks	
Instructor's Signature with Date:	

LAB SESSION 10

OBJECTIVE :

To analyze and study the operations of the following circuits:

- JK and Master-Slave JK Flip-Flop
- T Flip-Flop

THEORY:

So far you have encountered with *combinatorial logic*, i.e. circuits for which the output depends only on the inputs. In many instances it is desirable to have the next output depending on the current output. A simple example is a *counter*, where the next number to be output is determined by the current number stored. Circuits that remember their current output or state are often called *sequential logic* circuits. Clearly, sequential logic requires the ability to store the current state. In other words, *memory* is required by sequential logic circuits, which can be created with boolean gates. If you arrange the gates correctly, they will remember an input value. This simple concept is the basis of RAM (random access memory) in computers, and also makes it possible to create a wide variety of other useful circuits.

Memory relies on a concept called **feedback**. That is, the output of a gate is fed back into the input. The simplest possible feedback circuit using two inverters is shown below (Fig.1):

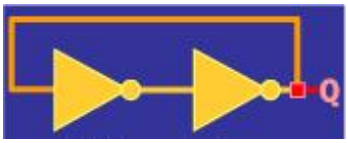
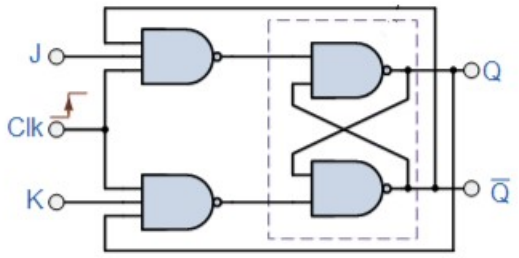


Fig.1: Simplest realization of feedback circuit

If you follow the feedback path, you can see that if Q happens to be 1 (or 0), it will always be 1 (or 0) . Since it's nice to be able to control the circuits we create, this one doesn't have much use -- but it does let you see how feedback works. It turns out that in "real" sequential circuits, you can actually use this sort of simple inverter feedback approach. The memory elements in these circuits are called *flip-flops*. A flip-flop circuit has two outputs, one for the normal value and one for the complement value of the stored bit. Binary information can enter a flip-flop in a variety of ways and gives rise to different types of flip-flops.

JK FLIP-FLOP:

The JK flip flop (JK means Jack Kilby, a Texas instrument engineer, who invented it) is the most versatile flip-flop, and the most commonly used flip flop. Like the RS flip-flop, it has two data inputs, J and K, and an EN/clock pulse input (CP). Note that in the following circuit diagram NAND gates are used instead of NOR gates. It has no undefined states, however. The fundamental difference of this device is the feedback paths to the AND gates of the input, i.e. Q is AND-ed with K and CP and Q' with J and CP.



Q_n	J	K	Q_{n+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1(Toggle.$\bar{Q}_n$)
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0(Toggle.$\bar{Q}_n$)

The JK flip-flop has the following characteristics:

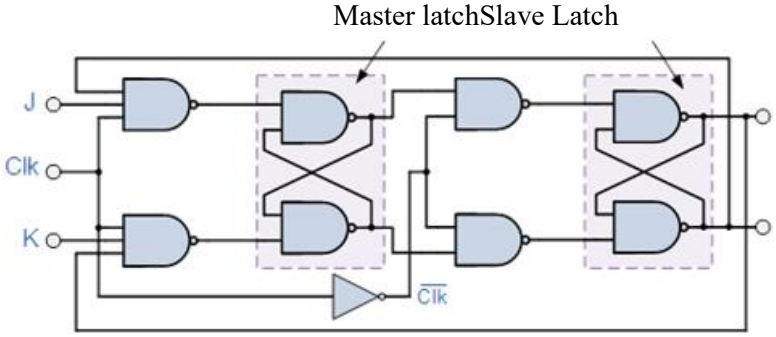
- If one input (J or K) is at logic 0, and the other is at logic 1, then the output is set or reset (by J and K respectively), just like the RS flip-flop.
- If both inputs are 0, then it remains in the same state as it was before the clock pulse occurred; again like the RS flip flop. CP has no effect on the output.
- If both inputs are high, however the flip-flop changes state whenever a clock pulse occurs; i.e., the clock pulse toggles the flip-flop again and again until the CP goes back to 0 as shown in the shaded rows of the characteristic table above. Since this condition is undesirable, it should be eliminated by an improvised form of this flip-flop as discussed in the next section.

MASTER-SLAVE JK FLIP-FLOP:

Although JK flip-flop is an improvement on the clocked SR flip-flop it still suffers from timing problems called "race" if the output Q changes state before the timing pulse of the clock input has time to go "OFF", so the timing pulse period (T) must be kept as short as possible (high frequency). As this is sometimes not possible with modern TTL IC's the much improved Master-Slave J-K Flip-Flop was developed. This eliminates all the timing problems by using two SR flip-flops connected together in series, one for the "Master" circuit, which triggers on the leading edge of the clock pulse and the other, the "Slave" circuit, which triggers on the falling edge of the clock pulse.

The master-slave JK flip flop consists of two flip flops arranged so that when the clock pulse enables the first, or master, it disables the second, or slave. When the clock changes state again (i.e., on its falling edge) the output of the master latch is transferred to the slave latch. Again, toggling is accomplished by the connection of the output with the input AND gates.

CIRCUIT DIAGRAM:



CHARACTERISTIC TABLE:

CP	J	K	Q_m	$\bar{Q}_m$	Q_n	$\bar{Q}_n$
0→1	0	0	Hold		Hold	
1→0	0	0	Hold		Hold	
0→1	0	1	0	1	Hold	
1→0	0	1	Hold		0	1
0→1	1	0	1	0	Hold	
1→0	1	0	Hold		1	0
0→1	1	1	Toggle		Hold	
1→0	1	1	Hold		Toggle	

T FLIP-FLOP:

The T flip-flop is a single input version of the JK flip-flop. The T flip-flop is obtained from the JK type if both inputs are tied together.

CIRCUIT DIAGRAM:

Same as Master-Slave JK flip-flop with J=K=1The toggle, or T, flip-flop is a bistable device, where the output of the T flip-flop "toggles" with each clock pulse.Till CP=0, the output is in hold state (three input AND gate principle).When CP=1, for T=0, previous output is memorized by the circuit. When T=1 along with the clock pulse, the output toggles from the previous value as given in the characteristic table below.

CHARACTERISTIC TABLE:

Qn	T	Qn+1
0	0	0
0	1	1
1	0	1
1	1	0

PROCEDURE:

1. Assemble the circuits one after another on your breadboard as per the circuit diagrams. Circuit diagrams given here do not show connections to power supply and LEDs assuming that you are already familiar with it from your previous lab experience.
2. Connect the ICs properly to power supply (pin 14) and ground (pin 7) following the schematics for ICs given above.
3. Using dip switch and resistors, facilitate all possible combinations of inputs from the power supply. Use the switch also to facilitate pulse input to the circuit.

4. Turn on power to your experimental circuit.
5. For each input combination, note the logic state of the normal and complementary outputs as indicated by the LEDs (ON = 1; OFF = 0), and record the results in a table.
6. Compare your results with the characteristic tables.
7. When you are done, turn off the power to your experimental circuit.

OBSERVATIONS:

Table for JK FF:

Table for Master-Slave JK FF:

Table for T FF:

RESULT:

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Psychomotor Domain Assessment Rubric-Level P3					
Skill Sets	Extent of Achievement				
	0	1	2	3	4
EquipmentIdentification Sensory skill to ***identify*** equipment and/or its component for a lab work.	Not able to identify the equipment.	--	--	--	Able to identify equipment as well as itscomponents.
Equipment Use Sensory skills to ***demonstrate*** the use of the equipment for the lab work.	Doesn't demonstrate the use of equipment.	Slightly demonstrates the use of equipment.	Somewhat demonstrates the use of equipment.	Moderately demon strates the use of equipment.	Fully demonstrates the use of equipment.
Procedural Skills ***Displays*** skills to act upon sequence of steps in lab work.	Not able to either learn or perform lab work procedure.	Able to slightly understand lab work procedure and perform lab work.	Able to somewhat understand lab work procedure and perform lab work.	Able to moderately understand lab work procedure and perform lab work.	Able to fully understand lab work procedure and perform lab work.
Response Ability to ***imitate*** the lab work on his/her own.	Not able to imitate the lab work.	Able to slightly imitate the lab work.	Able to somewhat imitate the lab work.	Able to moderately imitate the lab work.	Able to fully imitate the lab work.
Observation's Use*Displays* skills to use the observations from lab work for experimental verifications and illustrations.	Not able to use the observations from lab work for experimental verifications and illustrations.	Slightly able to use the observations from lab work for experimental verifications and illustrations.	Somewhat able to use the observations from lab work for experimental verifications and illustrations.	Moderately able to use the observations from lab work for experimental verifications and illustrations.	Fully able to use the observations from lab work for experimental verifications and illustrations.
Safety Adherence Adherence to ***safety*** procedures.	Doesn't adhere to safety procedures.	Slightly adheres to safety procedures.	Somewhat adheres to safety procedures.	Moderately adheres to safety procedures.	Fully adheres to safety procedures.
Equipment Handling*Equipment care* during the use.	Doesn't handle equipment with required care.	Rarely handles equipment with required care.	Occasionally handles equipment with required care.	Often handles equipment with required care.	Handles equipment with required care.
Group Work ***Contributes*** in a group based lab work.	Doesn't participate and contribute.	Slightly participates and contributes.	Somewhat participates and contributes.	Moderately participates and contributes.	Fully participates and contributes.

Laboratory Session No. _____ Date: _____

Weighted CLO (Psychomotor Score)	
Remarks	
Instructor's Signature with Date:	

LAB SESSION11

OBJECTIVE :

- Able to write synthesizable code of sequential circuits.
- Able to simulate the sequential circuit Verilog code on ModelSim or QuestaSim (Intel Edition).
- Able to synthesize the sequential circuit Verilog code and burn it in FPGA using Intel Quartus Prime.

PRE-LAB TASKS:

- Review the class lecture regarding Verilog coding for sequential circuits.
- Review the lecture regarding Quartus and Model Sim.
- Read sections 4.4 of the reference book [1].
- Read sections 7.8 and 7.9 of the reference book [2].
- Under the operation of 74160 IC from its data sheet.
- Download the DE1-SoC manual and understand the pin configuration of switches and LEDs.

EQUIPMENT/SOFTWARE REQUIRED:

- Intel Quartus Prime (Lite Edition)
- Questa or ModelSim (Intel Edition)
- FPGA Board (DE-1SoC Board)

TASKS

Task1: Implement an 8-bit Shift Register with parallel load capability and asynchronous reset on FPGA.

A. Write the synthesizable Verilog code of the task.

B. Simulate the verilog code on ModelSim (Intel Edition) and functionally verify your design.

C. Synthesize the verilog code and burn it on FPGA.

D. Physically verify design on FPGA.

Task 2: Implement the 4-bit counter on FPGA that mimic the functionality of 74160 Counter IC.

A. Write the synthesizable Verilog code of the task.

B. Simulate the verilog code on ModelSim (Intel Edition) and functionally verify your design.

C. Synthesize the verilog code and burn it on FPGA.

D. Physically verify design on FPGA.

Reference Book:

[1] Harris, Sarah L., and David Harris. Digital Design and Computer Architecture, RISC-V Edition. Morgan Kaufmann, 2021.
[2] Brown, Stephen. "Fundamentals of digital logic design with VHDL.", 3rd ed, 2010

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Psychomotor Domain Assessment Rubric-Level P3					
Skill Sets	Extent of Achievement				
	0	1	2	3	4
EquipmentIdentification Sensory skill to ***identify*** equipment and/or its component for a lab work.	Not able to identify the equipment.	--	--	--	Able to identify equipment as well as itscomponents.
Equipment Use Sensory skills to ***demonstrate*** the use of the equipment for the lab work.	Doesn't demonstrate the use of equipment.	Slightly demonstrates the use of equipment.	Somewhat demonstrates the use of equipment.	Moderately demon strates the use of equipment.	Fully demonstrates the use of equipment.
Procedural Skills ***Displays*** skills to act upon sequence of steps in lab work.	Not able to either learn or perform lab work procedure.	Able to slightly understand lab work procedure and perform lab work.	Able to somewhat understand lab work procedure and perform lab work.	Able to moderately understand lab work procedure and perform lab work.	Able to fully understand lab work procedure and perform lab work.
Response Ability to ***imitate*** the lab work on his/her own.	Not able to imitate the lab work.	Able to slightly imitate the lab work.	Able to somewhat imitate the lab work.	Able to moderately imitate the lab work.	Able to fully imitate the lab work.
Observation's Use*Displays* skills to use the observations from lab work for experimental verifications and illustrations.	Not able to use the observations from lab work for experimental verifications and illustrations.	Slightly able to use the observations from lab work for experimental verifications and illustrations.	Somewhat able to use the observations from lab work for experimental verifications and illustrations.	Moderately able to use the observations from lab work for experimental verifications and illustrations.	Fully able to use the observations from lab work for experimental verifications and illustrations.
Safety Adherence Adherence to ***safety*** procedures.	Doesn't adhere to safety procedures.	Slightly adheres to safety procedures.	Somewhat adheres to safety procedures.	Moderately adheres to safety procedures.	Fully adheres to safety procedures.
Equipment Handling*Equipment care* during the use.	Doesn't handle equipment with required care.	Rarely handles equipment with required care.	Occasionally handles equipment with required care.	Often handles equipment with required care.	Handles equipment with required care.
Group Work ***Contributes*** in a group based lab work.	Doesn't participate and contribute.	Slightly participates and contributes.	Somewhat participates and contributes.	Moderately participates and contributes.	Fully participates and contributes.

Laboratory Session No. _____ Date: _____

Weighted CLO (Psychomotor Score)	
Remarks	
Instructor's Signature with Date:	

LAB SESSION12

OBJECTIVE :

Able to write synthesizable code of Combinational circuits using processes.

PRE-LAB TASKS:

- Review the class lecture regarding Verilog coding using processes.
- Review the lecture regarding Quartus and Model Sim.
- Read sections 4.5 of the reference book [1].
- Complete Lab Session 04 of the manual.
- Complete Lab Session 05 of the manual.
- Download the DE1-SoC manual and understand the pin configuration of switches and LEDs.

EQUIPMENT/SOFTWARE REQUIRED:

- Intel Quartus Prime (Lite Edition)
- Questa or ModelSim (Intel Edition)
- FPGA Board (DE-1SoC Board)

TASKS

Task1: Implement a BCD to 7-Segment Decoder on FPGA.

A. Write the synthesizable Verilog code of the task.

B. Simulate the verilog code on ModelSim (Intel Edition) and functionally verify your design.

C. Synthesized the verilog code and burn it on FPGA.

D. To physically verify the design, connect the DE1 SoC board switches to inputs of the decoder where its outputs are connected 7-Segment display on the board.

Task2: Implement a 6 to 1 MUX on FPGA.

A. Write the synthesizable Verilog code of the task.

B. Simulate the verilog code on ModelSim (Intel Edition) and functionally verify your design.

C. Synthesized the verilog code and burn it on FPGA.

D. Physically verify design on FPGA.

Task3: Implement a 6 to 1 DE-MUX on FPGA.

A. Write the synthesizable Verilog code of the task.

B. Simulate the verilog code on ModelSim (Intel Edition) and functionally verify your design.

C. Synthesized the verilog code and burn it on FPGA.

D. Physically verify design on FPGA.

Reference Book:

[1] Harris, Sarah L., and David Harris. Digital Design and Computer Architecture, RISC-V Edition. Morgan Kaufmann, 2021.

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Psychomotor Domain Assessment Rubric-Level P3					
Skill Sets	Extent of Achievement				
	0	1	2	3	4
EquipmentIdentification Sensory skill to ***identify*** equipment and/or its component for a lab work.	Not able to identify the equipment.	--	--	--	Able to identify equipment as well as itscomponents.
Equipment Use Sensory skills to ***demonstrate*** the use of the equipment for the lab work.	Doesn't demonstrate the use of equipment.	Slightly demonstrates the use of equipment.	Somewhat demonstrates the use of equipment.	Moderately demon strates the use of equipment.	Fully demonstrates the use of equipment.
Procedural Skills ***Displays*** skills to act upon sequence of steps in lab work.	Not able to either learn or perform lab work procedure.	Able to slightly understand lab work procedure and perform lab work.	Able to somewhat understand lab work procedure and perform lab work.	Able to moderately understand lab work procedure and perform lab work.	Able to fully understand lab work procedure and perform lab work.
Response Ability to ***imitate*** the lab work on his/her own.	Not able to imitate the lab work.	Able to slightly imitate the lab work.	Able to somewhat imitate the lab work.	Able to moderately imitate the lab work.	Able to fully imitate the lab work.
Observation's Use*Displays* skills to use the observations from lab work for experimental verifications and illustrations.	Not able to use the observations from lab work for experimental verifications and illustrations.	Slightly able to use the observations from lab work for experimental verifications and illustrations.	Somewhat able to use the observations from lab work for experimental verifications and illustrations.	Moderately able to use the observations from lab work for experimental verifications and illustrations.	Fully able to use the observations from lab work for experimental verifications and illustrations.
Safety Adherence Adherence to ***safety*** procedures.	Doesn't adhere to safety procedures.	Slightly adheres to safety procedures.	Somewhat adheres to safety procedures.	Moderately adheres to safety procedures.	Fully adheres to safety procedures.
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Laboratory Session No. _____ Date: _____

Weighted CLO (Psychomotor Score)	
Remarks	
Instructor's Signature with Date:	

LAB SESSION 13

Problem Description:

Design and implement a sequence detector that meets the following specifications:

- The detector contains single input 'w' and output 'z'.
- All changes in the circuit occur on the positive edge of a clock signal.
- The output 'z' is equal to '1' if input 'w' receives sequence "01111110" in the immediately preceding clock cycles.

Requirement of Lab Session Completion:

- The design solution must include state diagrams, state tables, and the final circuit consisting of flip-flops and logic gates.
- In addition design solution must also clearly mention all the assumptions taken during the design.
- Implementation of the design on a breadboard using flip-flop and logic gate IC.
- Write the synthesizable Verilog code for the design.
- Simulate the Verilog code for functional verification using Modelsim/Questasim.
- Burn the code on FPGA and physically verify that the implementation meets the problem specification.

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Assessment Rubric for OEL

Criterion	Level of Attainment				
	Below Average (0)	**Average (1)**	**Good (2)**	**Very Good (3)**	**Excellent (4)**
Understanding and Analysis Ability to comprehend and analyze the Assigned Task	Totally unable to understand the task	Only know basic concepts do not understand the assigned task	Somehow understand the problem but unable to analyze	Able to partly understand and analyze the assigned task	Fully understand and able to analyze the assigned task
Solution Ability to determine the solution for the Assigned Task	Unable to determine the solution	Able to understand some basic concepts but unable to connect them to get a solution	Partly solve the problems	Able to solve the problem with minor errors	Able to solve completely
Response Ability to answer questions related to the Assigned Task	Unable to answer any questions	Able to answer only few basic questions	Able to answer almost half of the questions	Able to answer most of the questions	Able to answer all questions

Student's Name: _____ Roll No.: _____

Total Score = _____

Instructor's Signature: _____