Department of Telecommunications Engineering

NED University of Engineering & Technology

LABORATORY WORKBOOK

For the Course

DIGITAL COMMUNICATION AND INFORMATION THEORY

(TC-311)

Instructor Name: ______________________________

Student Name: ______________________________

Roll Number: ________________ **Batch:** ____________

Semester: ________________ **Year:** ____________

Department: ______________________________

LABORATORY WORK BOOK

For The Course

DIGITAL COMMUNICATION AND INFORMATION THEORY

(TC-311)

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The Board of Studies of Department of Telecommunications Engineering

INTRODUCTION

Digital Communication and Information Theory Practical Workbook covers broad range of practicals that describes how to set up the digital communication experimental system, and provides explanations of principles and methods. We tried our best to relate what you are learning in class with what you are taking in the lab.

The practicals of this manual are arranged on modern trainer boards and the objectives are clearly defined. Some of the practicals are based on MATLAB to give an insight of the system design, analysis and simulation in the communication area.

You are required to go through the lab notebook and the suggested reading before coming to the lab. Make sure you bring with you the assignments and lab tasks, neat and tidy presented and enough explanatory for the marks to be awarded failing to which shall result in the deduction of marks. It must have the following:

- Objective
- Clear theoretical concepts & equations used, source code and results of the simulations or plotted data.
- Description of the results or data collected and plotted.
- Conclusions

You are supposed to fill in the observation and the result field at the time of the performance of the experiment and submit it then, get it duly signed and marked.

Each lab task is due until the next lab session.

Recommended readings for each laboratory session:

[1] Haykin, S, *Communication Systems*, John Wiley & Sons, 4th Edition.
[2] Proakis, John G., *Digital Communications*, New York, McGraw-Hill, 3rd Edition.
[3] Sklar, Bernard, *Digital Communications: Fundamentals and Applications*, Englewood Cliffs, N.J., Prentice-Hall,2nd Edition.
[4] Tomasi, W, *Advanced Electronic Communications Systems*, Prentice-Hall International, 5th Edition.

CONTENTS

Lab No.	Date	Experiment	CLOs	Pg. No.	Remarks/ Signature
1		• To analyze ‘Pulse Amplitude Modulation’ and Sample and Hold’ methods of sampling and to observe the Aliasing effect.	03	3	
2		• To demonstrate transmission of information at different information rate • To show relationship between information rate and frequency spectrum	03	11	
3		• To demonstrate Quantization • To demonstrate Binary Coding	03	16	
4		• To analyze RZ (Return to zero) and NRZ (Not Return to zero) digital data formats.	03	20	
5		• To demonstrate MANCHESTER and AMI digital data formatting	03	26	
6		• To demonstrate word synchronization in digital data transmission	03	32	
7		• To demonstrate Amplitude Shift Keying (ASK) modulation and demodulation.	03	35	
8		• To demonstrate Frequency Shift Keying (FSK) modulation and demodulation.	03	38	
9		• To demonstrate the 2 PSK (Phase Shift Keying) modulation and demodulation.	03	41	
10		• Analysis of Costas Loop for coherent detection at the receiver	03	45	
11		• To analyze QPSK modulation & demodulation.	03	49	
12		• To analyze DPSK Modulation and Demodulation.	03	55	
13		• To implement image compression algorithm using simulation software	03	60	

LAB SESSION 01

Objective:

- To demonstrate ‘pulse amplitude modulation’ and ‘sample and hold’ methods of sampling and to observe the aliasing effect.

Equipment required:

Digital data formatting work board 53-150 which comprises the following blocks:

- Signal generator
- Compressor
- Filter
- Pam generator
- Sample and hold circuit
- Analogue to digital converter
- Nrz, rz, bprz, sp, ami links
- Synchronization circuits
- Digital to analogue converter
- Expander

Theory:

Sampling:

Pulse amplitude modulation is achieved by multiplying the signal waveform with a square Wave of a higher frequency.

This results in a waveform similar to the one below.

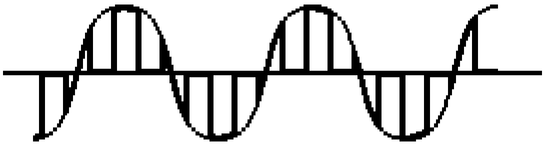


Figure 1.1

If, in the frequency domain, the source signal looks something like this:

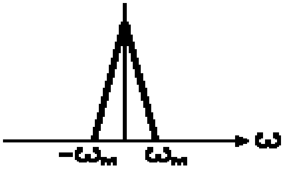


Figure 1.2

And the square wave looks like this ...

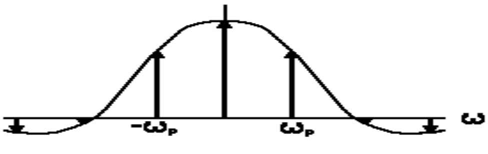


Figure 1.3

Then the spectrum of the pam signal will look like this:

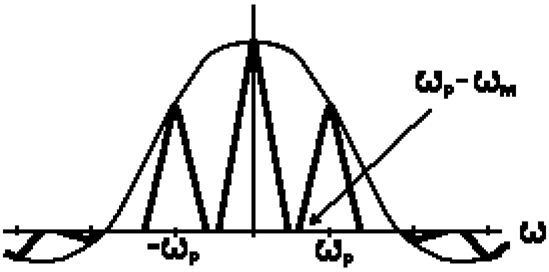


Figure 1.4

From this we can see that the original signal can be recovered exactly from the pam signal simply by filtering out the higher frequency components of the signal with a low pass filter.

However, there is a condition that must be satisfied for this to be possible. The filtering will not work if the harmonic components of the modulated waveform are not sufficiently far from the baseband component that the two do not overlap.

I.e., $(\omega_p - \omega_m) > \omega_m$ must be true.

This leads to the conclusion that $\omega_p > 2\omega_m$

In other words, for the original signal to be correctly recovered by low pass filtering, the sampling square wave frequency must be greater than twice the highest frequency component in the signal that is being sampled.

The value of $2\omega_m$ is called the nyquist frequency.

If the signal is sampled at a frequency less that the nyquist frequency for that signal, the baseband and harmonics overlap, and aliasing occurs.

It is interesting to note that it is only the frequency of the sampling square wave that effects the recoverability of the original signal, not the mark space ratio.

The 'on' time of the square wave will only effect the size of the signal after the low pass filter - the shorter the 'on' time, the smaller the recovered signal.

<u>Pulse amplitude modulation:</u>

A pulse amplitude modulated signal is a signal that has had a proportion of its waveform removed at regular intervals leaving behind a series of pulses whose amplitudes describe the original waveform.

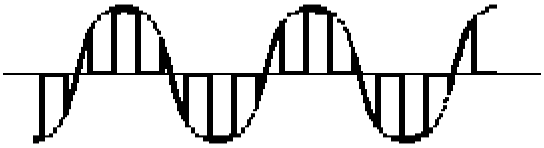


Figure 1.5

The original modulated waveform can be extracted from the PAM signal by simply passing it through a low pass filter which soothes out the pulses.

Pulse Amplitude Modulation is produced by multiplying a signal with a square wave of constant amplitude.

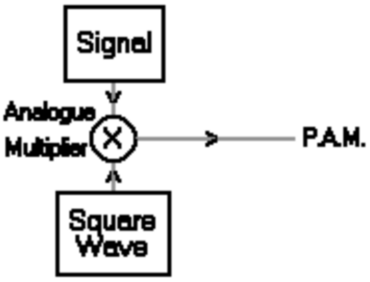


Figure 1.6: PAM Sampling

At the points where the square wave has zero amplitude, the resultant PAM signal will also have zero amplitude.

At the points where the square wave peaks, the PAM signal will have the shape of the original signal, with an amplitude that is dependent on the instantaneous value of the signal.

In the portions of the PAM waveform where there is zero amplitude, there is no information about the waveform carried.

These gaps in the waveform can be filled by the information carrying portions of another completely different PAM waveform. This is a technique called multiplexing.

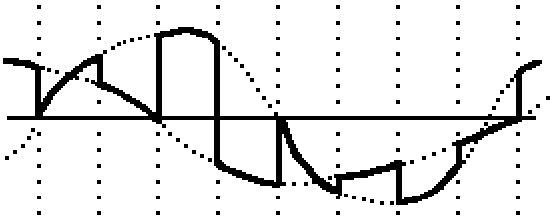


Figure 1.7

The single waveform made up of two PAM signals can be transmitted over a communications link and split up again, or demultiplexed, at the receiver into the two separate PAM waveforms.

These waveforms can then be filtered to reproduce the two original signals, having been transmitted using the space required for just one of them.

A sine wave signal is multiplied by a square wave sampling signal using an analogue multiplier circuit to produce a PAM signal. The frequency of the original signal can be altered. The sampling signal has been arranged to be at the frequency needed to chop up the signal into eight pulses per cycle of its sine wave.

Sample and Hold:

A waveform can be represented by a sequence of pulses, `snapshots` of the waveform at
equally spaced intervals. These pulses are known as samples. Provided that there are enough samples, i.e., that the sample frequency is high enough, the original signal can be completely recovered from its sampled equivalent.

To restore a PAM signal, it is only necessary to sample the PAM waveform when it is non-zero, and then filter the sampled waveform to reproduce the original signal. To make the recovered signal less vulnerable to noise it is useful to hold the last sample until the next one is taken. This is known as sample and hold.

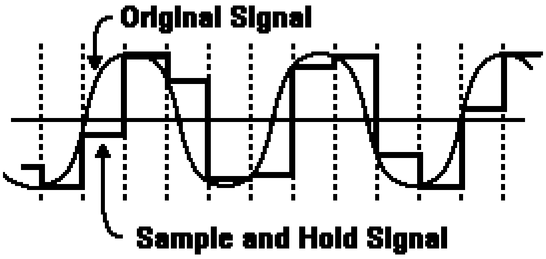


Figure 1.8

A signal is sampled by connecting it quickly to a capacitor via a switch. While the signal is connected, the capacitor is charged until it soon reaches the level of the signal. The time constant of the charging circuit is made as small as possible so that the time taken to reach the signal level is minimal.

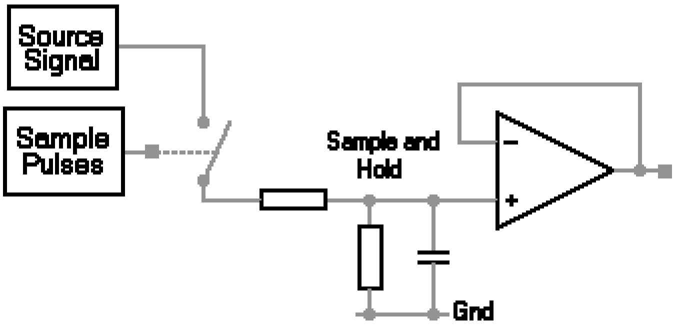


Figure 1.9: Sample and Hold Circuit

When the switch disconnects the signal from the capacitor, the level that the capacitor had reached at that point is held due to the high impedance input of the buffer amplifier.

The waveform that is seen at the output of the buffer amplifier resembles a series of steps, the leading edges of which are rounded off due to the capacitor being charged to the next level at this point.

In the practical you will examine a PAM signal which is sampled by a sample and hold circuit. This circuit is driven by a periodic sample pulse at the sample frequency. The sample frequency is matched automatically to the frequency of the PAM signal's pulses. The PAM signal can be changed in frequency, and the length of the sample pulse can be altered.

Aliasing:

A waveform can be represented by a sampled waveform made up of samples of the original signal taken at equally spaced intervals. Provided that there are enough samples, ie. That the sample frequency is high enough, the original signal can be completely recovered from its sampled equivalent.

If the samples are not taken at a high enough rate, the original waveform cannot be recovered because aliasing occurs.

To ensure that the sampled signal contains enough information to enable the original signal to be regenerated without distortion, the frequency at which samples are taken needs to be at least twice that of the highest frequency component in the original signal.

This minimum sampling frequency is called the Nyquist frequency.

If samples are taken at slightly less than the Nyquist frequency, aliasing occurs. The result of this is that the recovered signal appears to be one of much lower frequency, as shown below.

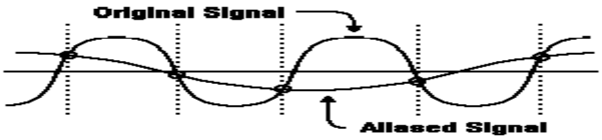
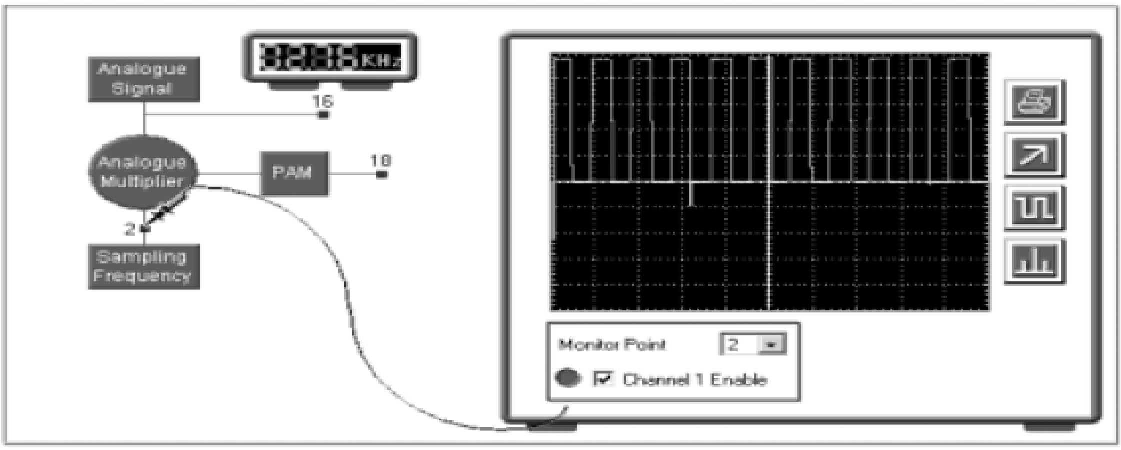


Figure 1.10

Procedure:

Pulse amplitude modulation:

Set all of the potentiometer controls to their mid positions. Observe the analogue source signal monitor point **16**, the sampling square wave monitor point 2 and the pulse amplitude modulated signal monitor point **18**. Use the oscilloscope and spectrum analyzer to compare these signals. Alter the analogue source, **signal frequency (2)** and **signal level (1)**, controls and observe the results.



Monitor Point 2

● ☑ Channel 1 Enable

Figure 1.11

Observations and results:

Set the **signal frequency (2)** and **signal level (1)** controls to their mid positions.

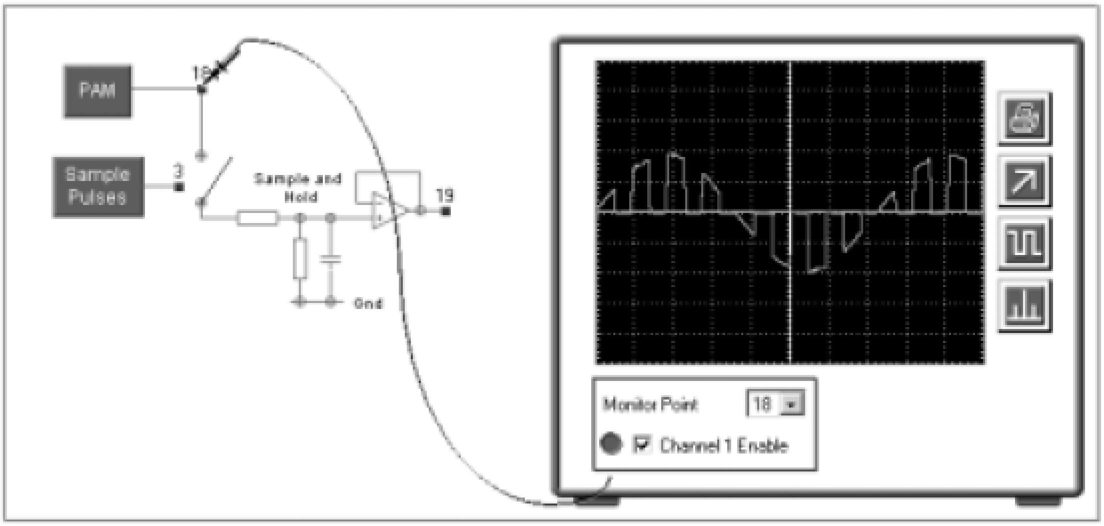
(a) Use the large display to compare the frequency spectrums of the input sine wave, the sampling signal and the pam signal. Can you identify any similarities between them?

(b) Why are there two peaks on the pam spectrum at the positions where there are single peaks on the sampling square wave spectrum?

(c) What would happen to the pairs of peaks on the pam spectrum if the sampling frequency remained the same, and the source signal frequency was increased?

Sample and hold:

Observe the pam signal monitor point 18 using the oscilloscope. Vary the **signal frequency (2)** and the **signal level (1)** controls. Observe the sample pulses monitor point **3**. Investigate the effect of altering the **sample time (4)** control.



Monitor Point 18

● ☑ Channel 1 Enable

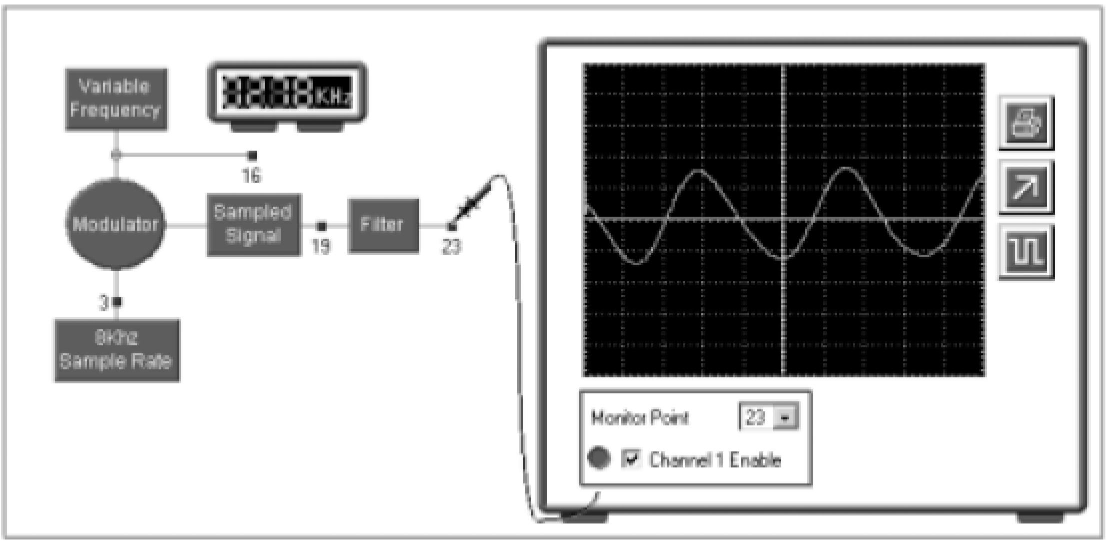
Figure 1.12

Observations and results:

(a) Why is there a buffer amplifier at the output of the sample and hold circuit?
(b) What happens when the sample time is very short?
(c) Why does this happen?
(d) What happens when the sample time is long and the frequency of the PAM signal is high?
(e) Why do you think this happens?
(f) What can you say about the ideal requirements for the sample and hold circuit in terms of its sample time and its charging time constant?

Aliasing:

Set all of the potentiometer controls to their mid positions. Observe the analogue source signal monitor point **16** , the Sampled Signal monitor point **19** and the Filter output monitor point **23** with the oscilloscope. Adjust the **Signal frequency (2)** control over its whole range and examine the resulting sampled signals.



Monitor Point 23

● ☑ Channel 1 Enable

Figure 1.13

Observations and results:

(a) Slowly sweep the frequency control for the input signal to the modulator from minimum to maximum and observe the sampled output signal. Describe what happens to the output signal.
(b) When adjusting the frequency of the input signal the sampled output signal appears to become a square wave at a certain frequency. What is the frequency of the input signal when this occurs?
(c) What do you think is happening at this point?

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NED University of Engineering & Technology
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Course Code and Title: TC-311 Digital Communication and Information Theory

Laboratory Session No. _____________ Date: ______________________

Psychomotor Domain Assessment Rubric-Level P3

Skill Sets	Extent of Achievement				
	0	1	2	3	4
<u>Equipment</u> <u>Identification</u> Sensory skill to ***identify*** equipment and/or its component for a lab work.	Not able to identify the equipment.	--	--	--	Able to identify equipment as well as its components.
<u>Equipment Use</u> Sensory skills to ***demonstrate*** the use of the equipment for the lab work.	Doesn't demonstrate the use of equipment.	Slightly demonstrates the use of equipment.	Somewhat demonstrates the use of equipment.	Moderately demon strates the use of equipment.	Fully demonstrates the use of equipment.
<u>Procedural Skills</u> ***Displays*** skills to act upon sequence of steps in lab work.	Not able to either learn or perform lab work procedure.	Able to slightly understand lab work procedure and perform lab work.	Able to somewhat understand lab work procedure and perform lab work.	Able to moderately understand lab work procedure and perform lab work.	Able to fully understand lab work procedure and perform lab work.
<u>Response</u> Ability to ***imitate*** the lab work on his/her own.	Not able to imitate the lab work.	Able to slightly imitate the lab work.	Able to somewhat imitate the lab work.	Able to moderately imitate the lab work.	Able to fully imitate the lab work.
<u>Observation's Use</u> ***Displays*** skills to use the observations from lab work for experimental verifications and illustrations.	Not able to use the observations from lab work for experimental verifications and illustrations.	Slightly able to use the observations from lab work for experimental verifications and illustrations.	Somewhat able to use the observations from lab work for experimental verifications and illustrations.	Moderately able to use the observations from lab work for experimental verifications and illustrations.	Fully able to use the observations from lab work for experimental verifications and illustrations.
<u>Safety Adherence</u> Adherence to ***safety*** procedures.	Doesn't adhere to safety procedures.	Slightly adheres to safety procedures.	Somewhat adheres to safety procedures.	Moderately adheres to safety procedures.	Fully adheres to safety procedures.
<u>Equipment Handling</u> ***Equipment care*** during the use.	Doesn't handle equipment with required care.	Rarely handles equipment with required care.	Occasionally handles equipment with required care.	Often handles equipment with required care.	Handles equipment with required care.
<u>Group Work</u> ***Contributes*** in a group based lab work.	Doesn't participate and contribute.	Slightly participates and contributes.	Somewhat participates and contributes.	Moderately participates and contributes.	Fully participates and contributes.

Weighted CLO (Psychomotor Score)	
Remarks	
Instructor's Signature with Date:	

LAB SESSION 02

Information Transmission

Objective:

- To demonstrate transmission of information at different information rate
- To show relationship between information rate and frequency spectrum

Equipment required:

PCM and Link Analysis Workboard 53-170 which comprises the following blocks

- Signal Generators
- NRZ, RZ, BPRZ, SP, AMI Links
- Synchronization Circuits
- D to A convertor
- filter

Theory 2(a):

A communications system is used for communicating information, which originates from an information source The meaning, or lack of meaning, of the information is not important when dealing with communications systems, only the quantity of information and its integrity are important.

No information is transmitted by a continuous symbol.

Information requires change

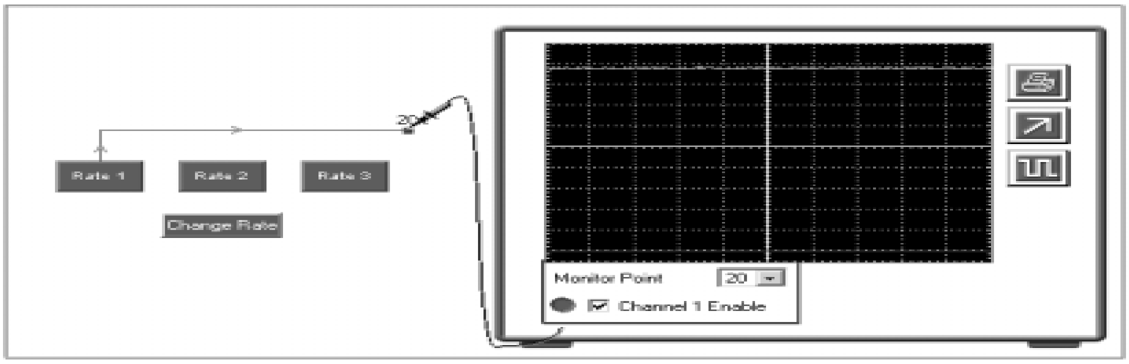
The simplest information system is binary, where the information is contained in the choice of one state out of two possible states, normally given the symbols 1 and 0.

These are binary digits (often shortened to 'bits'). One bit is the smallest division of binary information.

The bit is a division of information and the choice of 1 or 0 constitutes the information.

Procedure 2(a)

Set the ***PCM level control (4)*** and the ***PCM bandwidth control (5)*** to maximum. Set all the other controls to their mid positions. Consider the information sources shown below. Monitor their signals using the oscilloscope. Click on the ***Change Rate button*** to change between sources



Monitor Point 20

☑ Channel 1 Enable

Figure 2.1

Observations and Results

a) If the low state of a signal represents 0 and the high state 1, what form of information system does this represent?

b) What information is being carried by the signal with rate 1?

c) Does the signal with rate 2 carry any information?

d) Does the signal with rate 3 carry any information?

Theory 2(b)

Theoretically, a square waveform has a frequency spectrum that contains the fundamental frequency and all its odd harmonics up to infinity.

The magnitude of the harmonic components decreases as the order goes up; eg, the component at the third harmonic is larger than that at the fifth, and so on.

In practice, the number of harmonics that are considered to have a significant amplitude is limited to about nine, however, to convey a really sharp-edged square waveform requires a very wide bandwidth.
The number of binary digits (bits) that is transmitted in unit time (normally one second) is known as the **Information Transfer Rate**.

This is normally expressed in **bits**, or **kilobits**, per second. Another term often used

for this is the **Bit Rate**.

Signaling Rate

The **Signaling Rate** specifies how fast the signal states change in a communications channel.

This is normally expressed in **Bauds**. One baud is a rate of one change per second. Another term often used for this

is the **Baud Rate**.

Procedure 2(b)

The information sources below are the same as in the previous practical. Monitor their signals using the oscilloscope and spectrum analyzer (use the buttons to change instruments).

Pay particular attention to the bandwidths of the three signals when they are displayed on the spectrum analyzer.

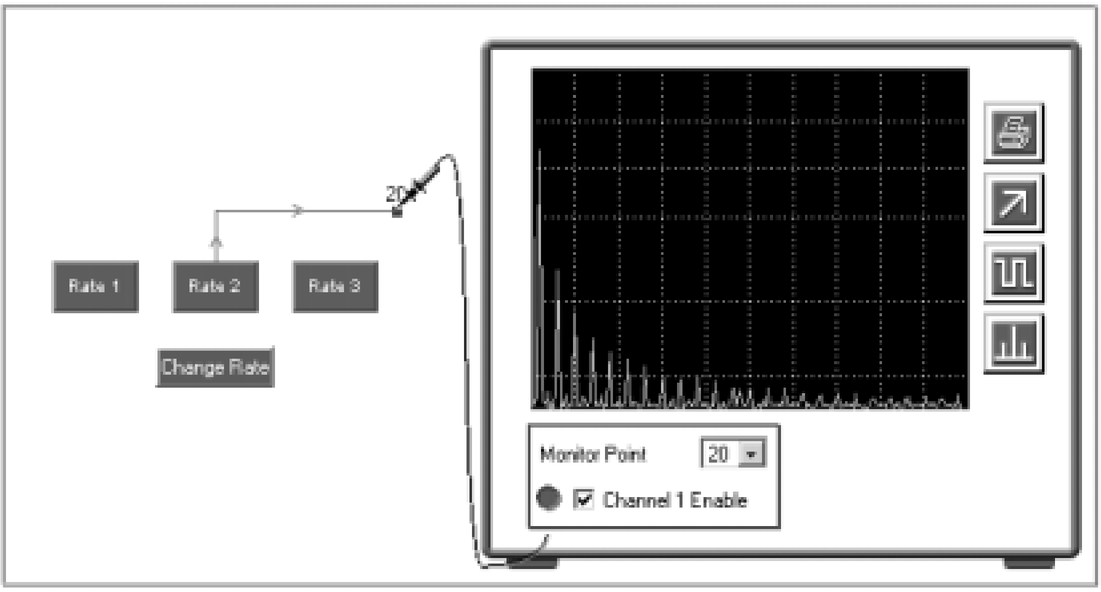


Figure 2.2

Observation and Results

a. What frequency components are present for the signal of rate 1?
b. Measure the period of the waveform of rate 2. What is the bit rate of this signal and in what units is it measured?
c. What is the bit rate of the waveform of rate 3?
d. How does this relate to the frequency components of the waveform as seen on the spectrum analyser?
e. Look at the spectrum on the large spectrum analyser. At about 160kHz, how do the magnitudes of the components of the signals at rates 2 and 3 compare?

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Weighted CLO (Psychomotor Score)	
Remarks	
Instructor's Signature with Date:	

LAB SESSION 03

A to D Conversion

Objective:

- To demonstrate Quantization
- To demonstrate Binary Coding

Equipment required:

Digital data formatting workboard 53-150 which comprises the following blocks:

- Signal generator
- Compressor
- Filter
- Pam generator
- Sample and hold circuit
- Analogue to digital converter
- Nrz, rz, bprz, sp, ami links
- Synchronization circuits
- Digital to analogue converter
- Expander

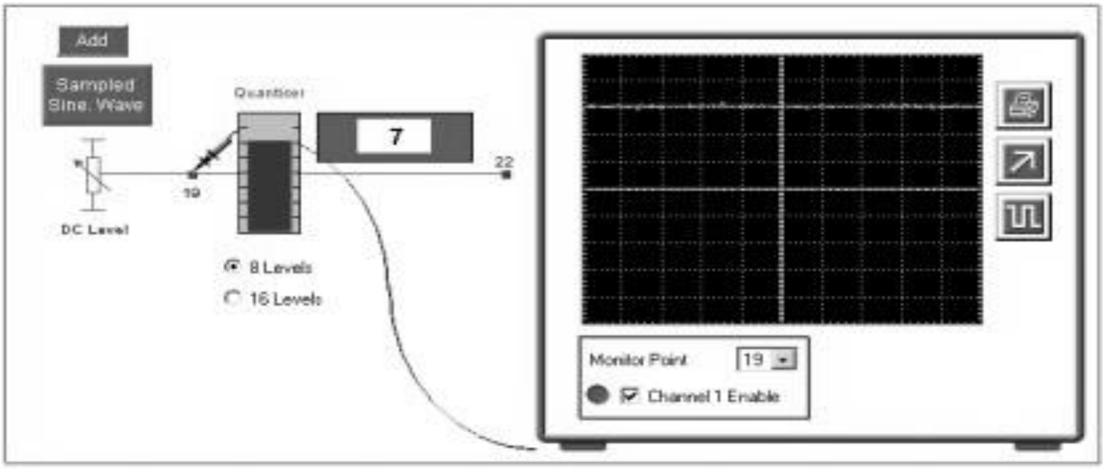
Theory 3(a):

In practice the pulse heights are assigned integer numbers. The range of possible heights is divided into equal sections and each pulse is measured against this. The process is called quantization.

In the practical you will see the effects of quantizing on a variable DC level and a sampled sine wave. The number of levels of quantization can be set to either eight or sixteen. The effective waveform before and after quantization has occurred can be observed on the oscilloscope

Procedure 3(a)

Observe the dc signal at monitor point ***19*** . Vary the level with the ***dc (5)*** control. Now look at monitor point ***22*** , the quantized output. Observe the operation of the quantizer. Now change the number of quantization levels to sixteen and note the result.



● 8 Levels

○ 16 Levels

Monitor Point 19

☑ Channel 1 Enable

Figure 3.1

Switch the quantize input to a sine wave signal. Adjust the ***Signal level (1)*** control while observing the signal at monitor point ***22*** . Switch the number of quantization levels to eight and again examine the quantized waveform monitor point ***22***

Observation and Results

a) With Eight levels and Sine wave selected, set the sampled ***Signal level (1)*** control for 1.4 V pk-pk (monitor point ***19***). Is the quantized signal (monitor point ***22***) a reasonable approximation to the input signal ?

b) Reduce the level of the input signal to 0.2 V pk-pk, with the number of quantizing levels still set to eight. Is the quantized signal still a reasonable approximation to the input signal ?

c) Increase the number of quantizing levels to sixteen. Does this make a difference to the quantized signal?

d) What can you say about the number of quantizing levels used and the distortion of the quantized signal?

Theory 3(b)

If the quantized signal is binary coded then the noise can further be reduced . In binary coding any quantized level will have value in form of zero or one as shown below

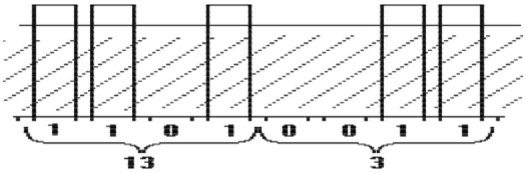


Figure 3.2

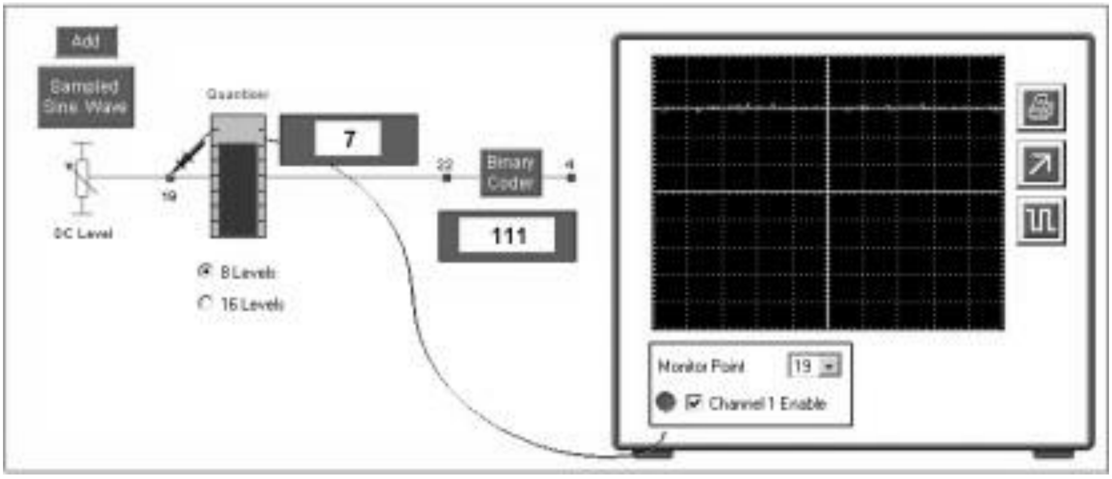
All that the receiver has to do is to decide whether each pulse is a '1' maximum amplitude pulse or a '0' zero amplitude pulse. The level of noise on the signal has to be very large before this information is corrupted.

For each sampled pulse in the original sampled waveform there must be several pulses in the binary coded quantized signal. For eight levels there must be three pulses per sample. For sixteen levels there must be four pulses per sample. For a good representation of speech waveforms, 256 levels of quantization are used. This requires eight pulses per sample.

In the practical you will see a quantizer as in the last practical. The output number from the quantizer is now used to generate a binary coded pulse train for each sample taken. This can be observed on the oscilloscope.

Procedure 3(b)

Use the same procedure as in the previous practical to examine the waveforms at monitor points ***19*** and ***22*** , observing the effect of the quantizer on a variable sine wave or variable dc level with eight or sixteen quantizing levels.



● 8 Levels

○ 16 Levels

Monitor Point 19

☑ Channel 1 Enable

Display the output at monitor point ***4*** to observe the binary sequence that is transmitted to represent the quantized levels.

Observation and Results

a) For eight quantising levels, how many bits are needed to code each sample?

b) How many are needed for sixteen quantizing levels?

c) How many would be required for 256 quantizing levels?

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NED University of Engineering & Technology
Department of Telecommunications Engineering
Course Code and Title: TC-311 Digital Communication and Information Theory
Laboratory Session No. _____________ Date: ______________________

Psychomotor Domain Assessment Rubric-Level P3					
Skill Sets	Extent of Achievement				
	0	1	2	3	4
Equipment Identification Sensory skill to ***identify*** equipment and/or its component for a lab work.	Not able to identify the equipment.	--	--	--	Able to identify equipment as well as its components.
Equipment Use Sensory skills to ***demonstrate*** the use of the equipment for the lab work.	Doesn't demonstrate the use of equipment.	Slightly demonstrates the use of equipment.	Somewhat demonstrates the use of equipment.	Moderately demonstrates the use of equipment.	Fully demonstrates the use of equipment.
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Observation's Use ***Displays*** skills to use the observations from lab work for experimental verifications and illustrations.	Not able to use the observations from lab work for experimental verifications and illustrations.	Slightly able to use the observations from lab work for experimental verifications and illustrations.	Somewhat able to use the observations from lab work for experimental verifications and illustrations.	Moderately able to use the observations from lab work for experimental verifications and illustrations.	Fully able to use the observations from lab work for experimental verifications and illustrations.
Safety Adherence Adherence to ***safety*** procedures.	Doesn't adhere to safety procedures.	Slightly adheres to safety procedures.	Somewhat adheres to safety procedures.	Moderately adheres to safety procedures.	Fully adheres to safety procedures.
Equipment Handling ***Equipment care*** during the use.	Doesn't handle equipment with required care.	Rarely handles equipment with required care.	Occasionally handles equipment with required care.	Often handles equipment with required care.	Handles equipment with required care.
Group Work ***Contributes*** in a group based lab work.	Doesn't participate and contribute.	Slightly participates and contributes.	Somewhat participates and contributes.	Moderately participates and contributes.	Fully participates and contributes.

Weighted CLO (Psychomotor Score)	
Remarks	
Instructor's Signature with Date:	

LAB SESSION 04

Binary Signaling Format

Objective:

- To demonstrate RZ (return to zero) and NRZ (not return to zero) digital data formating.

Equipment required:

Digital data formatting workboard 53-150 which comprises the following blocks:

- Signal generator
- Compressor
- Filter
- Pam generator
- Sample and hold circuit
- Analogue to digital converter
- Nrz, rz, bprz, sp, ami links
- Synchronization circuits
- Digital to analogue converter
- Expander

Theory:

A binary coded waveform can be represented by a number of different data formats using either unipolar or bipolar signals. Different data formats can be distinguished by the bandwidth required and the characteristics available for channel.

Different data formats have differing minimum bandwidths associated with them. The maximum number of bits that can be transmitted with a single high-low cycle is two for NRZ, and one for RZ, bi-phase, bipolar RZ and AMI i.e., NRZ can transmit 2 bps/hz (bits per second per hertz). The other formats can transmit 1 bps/hz.

The bps/hz term is called the bandwidth efficiency.

For a binary PCM system using *n* quantizing levels the minimum required bandwidth is*: b >= 1/2 (log2n / t)* where 1/t is the sample rate.

Binary data formats

(a) NRZ

An NRZ coded signal is high for '1' code bits and low for '0' code bits

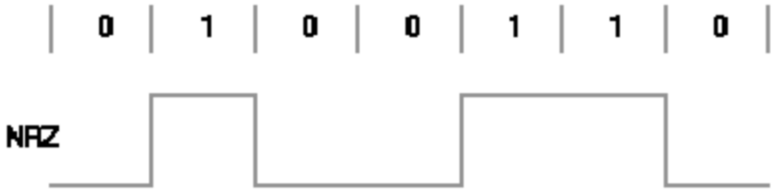

Figure 4.1 NRZ encoding

This is a very simple coding, as nothing needs to be done at all to the basic binary serial data.

Bit clock recovery

The NRZ signal contains no periodic component at the bit clock frequency. The rising and falling edges of the data are used to generate pulses. The pulses trigger a bit clock monostable which has an 'on' period approximately half that of the required bit clock frequency. The bit rate must be a known frequency, in this case 64kbits/sec.

The monostable pulses drive a phase locked loop, the VCO of which has its range centered on the required bit clock frequency. The pulses keep the vco locked in phase and frequency to the data. The PLL acts like a flywheel, keeping a stable, regular bit clock that is largely immune to jitter in the recovered signal that drives one of the phase comparator inputs.

The output of the VCO is the recovered bit clock.

Data recovery

The received data stream is integrated after it has been squared up by the threshold comparator. This is to minimize the effects of noise by summing the data over the whole bit period.

Just before the end of the bit period, the integrator output is sampled at a time determined by the recovered bit clock. This squared sampled data stream is the final recovered serial data.

Problems associated with NRZ

The nrz data format is not very good because:

- Its level drifts when it is used on an ac coupled link with data that has varying proportions of '1's and '0's in it. The threshold comparator in the receiver may mistakenly translate '1's as '0' or '0's as '1's if the signal's dc offset drifts too far.
- It does not have a regular level transition at the bit clock frequency, so a more complicated bit clock recovery process involving a bit clock monostable is required.
- For long streams of '1's or '0's, there are no level transitions in the data, so no monostable pulses are generated. This means that the PLL will receive no control signal for long periods and may drift out of lock, resulting in corruption of data.

The complexity of the bit clock and data recovery circuitry is important. Many receivers may be required not only at the end of the communications link, but also along its length, regenerating and retransmitting the weakened signal periodically. If the recovery processes require expensive or over complicated and hence more unreliable circuits then they will be less suitable for use as 'repeaters', which ideally should be cheap and require little maintenance.

Procedure:

Set all controls to mid position. Select the user data word or ADC data using the button and ***adjust dc (5)*** control to create a serial data word. Observe this at monitor point ***4*** . Select an ac or dc coupled link. Observe the coded data word before and after the link monitor points ***21*** & ***20.*** Note the signal offset for different data patterns for ac at monitor point ***20***.

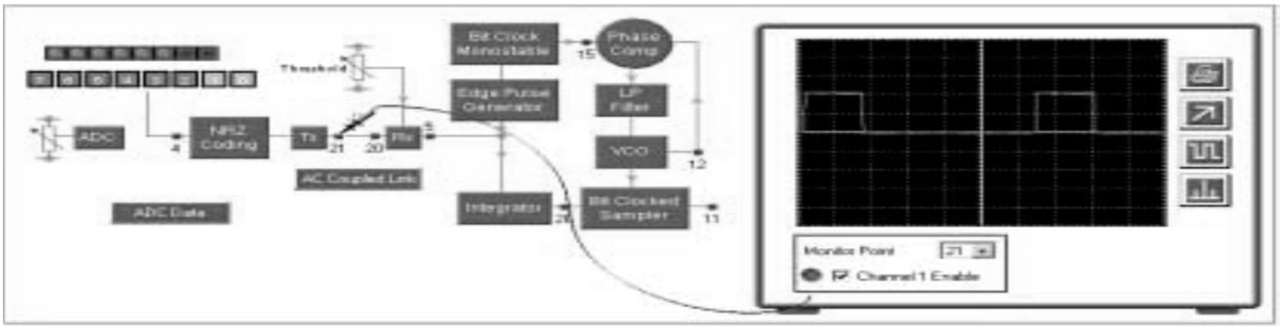

Figure 4.2

View the data at monitor point ***5*** . Adjust the ***receiver threshold (8)*** control for a stable signal. View the signals in the bit clock recovery circuit at monitor points ***15*** & ***12*** , adjust the ***synchronous bit clock (9)*** control for pll lock. Examine the signals in the data recovery path at monitor points ***26*** & ***11.*** Answer the questions provided. You will need to make some observations in order to answer them.

Observations and results:

(d) For an ac coupled link, what happens to the signal at monitor point ***20*** for various data words?
(e) Why is this a problem?
(f) What happens to the recovered bit clock for patterns of 00000000 and 11111111?
(g) Why is this a problem?

(b) RZ

A rz coded signal is high for '1' code bits and low for '0' code bits, but its level returns low half way through the bit period.

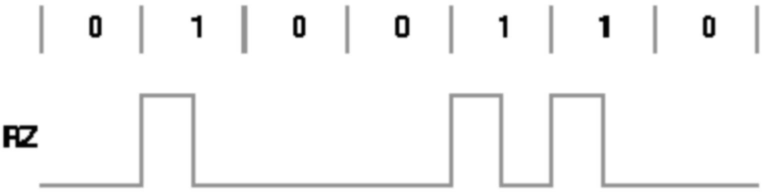

Figure 4.3 RZ encoding

This is a fairly simple coding. The basic binary serial data is and'ed with the transmitter bit clock to produce rz data. This means that the coded data contains a component at bit clock frequency which simplifies bit clock recovery.

Bit clock recovery

The squared data drives a phase locked loop, the VCO of which has its range centered on the required bit clock frequency. The pulses keep the VCO locked in phase and frequency to the data. The pll acts like a flywheel, keeping a stable, regular bit clock that is largely immune to jitter in the recovered signal that drives one of the phase comparator inputs. The output of the VCO is the recovered bit clock.

Data recovery

The received data stream is integrated after it has been squared up by the threshold comparator. This is to minimize the effects of noise by summing the data over the whole bit period. Just before the end of the middle of the bit period, the integrator output is sampled at a time determined by the recovered bit clock. This squared sampled data stream is the final recovered serial data.

Problems associated with rz

The RZ data format is not very good because:

- Its level drifts when it is used on an ac coupled link with data that has varying proportions of '1's and '0's in it. The threshold comparator in the receiver may mistakenly translate '1's as '0' or '0's as '1's if the signals dc offset drifts too far.
- For long streams of '0's, there are no level transitions in the data. This means that the pll will receive no control signal for long periods and may drift out of lock, resulting in corruption of data.

Procedure:

Set all controls to mid position. Select User Data Word or ADC Data using the button and adjust ***dc (5)*** control to create a serial data word. Observe this at monitor point ***4***. Select an AC or DC coupled link. Observe the coded data word before and after the link monitor points ***21*** & ***20.*** Note the signal offset for different data patterns for ac at monitor point ***20***.

View the data at monitor point **5.** Adjust the ***Receiver threshold (8)*** control for a stable signal. View the signals in the bit clock recovery circuit at monitor points ***15*** & ***12, adjust*** the ***Synchronous bit clock (9)*** control for PLL lock. Examine the signals in the data recovery path at monitor points ***26*** & ***11.*** Answer the questions provided. You will need to make some observations in order to answer them.

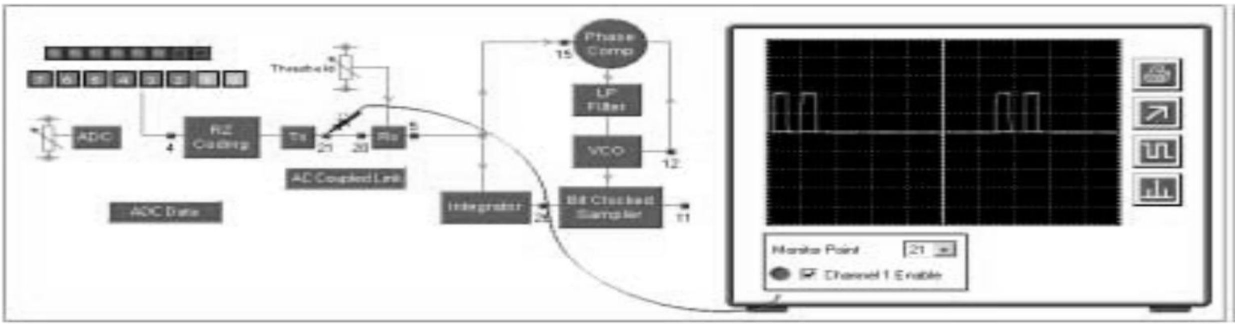

Figure 4.4

Observations and results:

1. On an AC coupled link, what happens to the signal at monitor point ***20*** for different data word patterns?
2. What happens to the ***bit clock*** for ***data words*** of:
    a. 11111111?
    b. 00000000?

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Psychomotor Domain Assessment Rubric-Level P3

Skill Sets	Extent of Achievement				
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Equipment Use Sensory skills to ***demonstrate*** the use of the equipment for the lab work.	Doesn't demonstrate the use of equipment.	Slightly demonstrates the use of equipment.	Somewhat demonstrates the use of equipment.	Moderately demon strates the use of equipment.	Fully demonstrates the use of equipment.
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Response Ability to ***imitate*** the lab work on his/her own.	Not able to imitate the lab work.	Able to slightly imitate the lab work.	Able to somewhat imitate the lab work.	Able to moderately imitate the lab work.	Able to fully imitate the lab work.
Observation's Use ***Displays*** skills to use the observations from lab work for experimental verifications and illustrations.	Not able to use the observations from lab work for experimental verifications and illustrations.	Slightly able to use the observations from lab work for experimental verifications and illustrations.	Somewhat able to use the observations from lab work for experimental verifications and illustrations.	Moderately able to use the observations from lab work for experimental verifications and illustrations.	Fully able to use the observations from lab work for experimental verifications and illustrations.
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Equipment Handling ***Equipment care*** during the use.	Doesn't handle equipment with required care.	Rarely handles equipment with required care.	Occasionally handles equipment with required care.	Often handles equipment with required care.	Handles equipment with required care.
Group Work ***Contributes*** in a group based lab work.	Doesn't participate and contribute.	Slightly participates and contributes.	Somewhat participates and contributes.	Moderately participates and contributes.	Fully participates and contributes.

Weighted CLO (Psychomotor Score)	
Remarks	
Instructor's Signature with Date:	

LAB SESSION 05

Binary Signaling Format

Objective:

- To demonstrate Manchester and AMI digital data formating.

Equipment required:

Digital Data Formating workboard 53-150 which comprises the following blocks:

- Signal generator
- Compressor
- Filter
- Pam generator
- Sample and hold circuit
- Analogue to digital converter
- Nrz, rz, bprz, sp, ami links
- Synchronization circuits
- Digital to analogue converter
- Expander

Theory:

A binary coded waveform can be represented by a number of different data formats using either unipolar or bipolar signals. Different data formats can be distinguished by the bandwidth required and the characteristics available for channel.

Different data formats have differing minimum bandwidths associated with them. The maximum number of bits that can be transmitted with a single high-low cycle is two for NRZ, and one for RZ, bi-phase, bipolar RZ and AMI i.e., NRZ can transmit 2 bps/Hz (bits per second per hertz). The other formats can transmit 1 bps/Hz.

The bps/Hz term is called the bandwidth efficiency.

For a binary PCM system using n quantizing levels the minimum required bandwidth is: $b >= 1/2 (\log 2n / t)$ where 1/t is the sample rate.

Binary data formats

(a) bi-phase (manchester)

A bi-phase coded signal is high for half a bit period then low for half a bit period for '1' code bits, and low for half a bit period then high for half a bit period for '0' code bits.

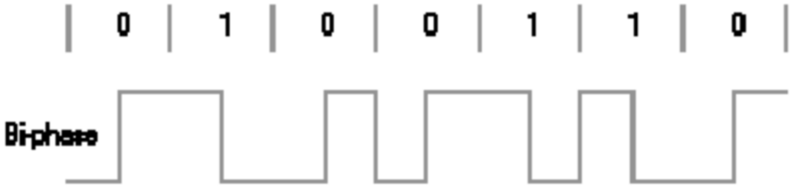


Figure 5.1 Manchester encoding

This is also a fairly simple coding; the basic binary serial data is xnored with the transmitter bit clock.

Bit clock recovery

The bi-phase signal has a periodic component at the bit clock frequency for most data patterns. However, a pattern of 10101010 will result in a square wave coded signal with a frequency of half the bit rate. To avoid problems, the rising and falling edges of the data are used to generate pulses for a bit clock monostable.

The pulses trigger the monostable which has an 'on' period approximately half that of the required bit clock frequency. The bit rate must be a known frequency, in this case 64kbits/sec.

The monostable pulses drive a phase locked loop, the vco of which has its range centred on the required bit clock frequency. The pulses keep the vco locked in phase and frequency to the data. The pll acts like a flywheel, keeping a stable, regular bit clock that is largely immune to jitter in the recovered signal that drives one of the phase comparator inputs.

The output of the vco is the recovered bit clock.

Data recovery

After it has been squared up by the threshold comparator, the received data stream is xor’ed with the receiver bit clock. It is then integrated to minimize the effects of noise by summing the data over the whole bit period.

Just before the end of the bit period, the integrator output is sampled at a time determined by the recovered bit clock. This squared sampled data stream is the final recovered serial data.

Problems associated with bi-phase coding

The bi-phase data format is not so bad, although:

- It does not have a regular level transition at the bit clock frequency, so a more complicated bit clock recovery process involving a bit clock monostable is required.

Procedure:

Set all controls to mid position. Select user data word or adc data using the button and adjust ***dc (5)*** control to create a serial data word. Observe this at monitor point ***4***. Select an ac or dc coupled link. Observe the coded data word before and after the link monitor points ***21*** & ***20***. Note the signal offset for different data patterns for ac at monitor point ***20.***

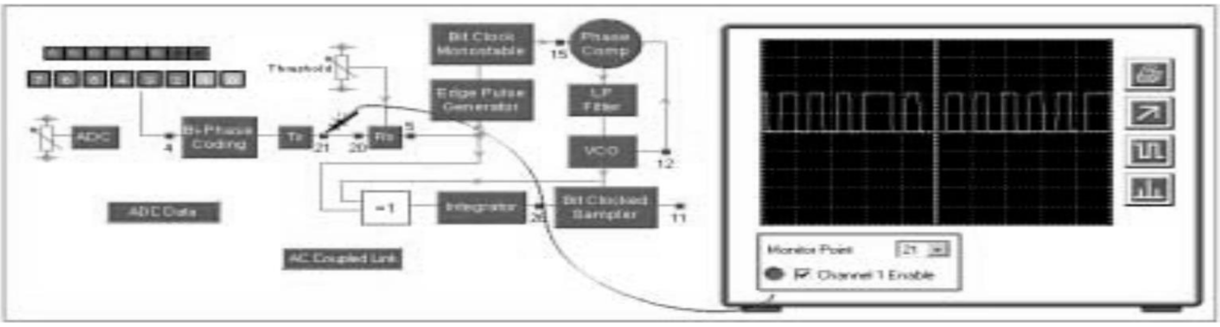


Figure 5.2

View the data at monitor point ***5.*** Adjust the ***receiver threshold (8)*** control for a stable signal. View the signals in the bit clock recovery circuit at monitor points ***15*** & ***12*** , adjust the ***synchronous bit clock (9)*** control for pll lock. Examine the signals in the data recovery path at monitor points ***26*** & ***11.*** Answer the questions provided. You will need to make some observations in order to answer them.

Observations and results:

1. Why is there no change in the level of the signal at monitor point ***20*** for dc and ac coupled links with different data words?
2. What happens to the signals at monitor points ***12*** and ***15*** for data words of:
    a. 11111111?
    b. 00000000?
    c. 10101010?

(b) Ami (ternary)

AN AMI coded signal is low for '0' code bits and alternately positive or negative for half a bit period then zero for half a bit period for '1' code bits.

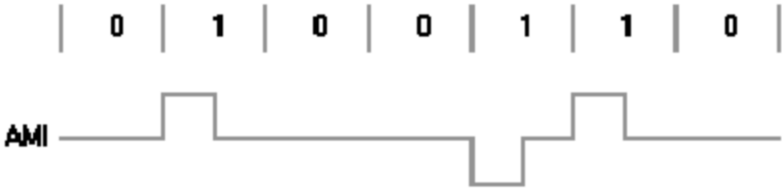


Figure 5.3 AMI encoding

Bit clock recovery

The AMI signal contains a component at the bit clock frequency. The receiver has positive and negative threshold outputs for the positive and negative '1's. These two outputs are xored to produce a stream of pulses at the bit clock rate. However, there will be gaps in the waveform for '0's in the data stream. The stream of pulses drives a phase locked loop, the VCO of which has its range centered on the required bit clock frequency. The pulses keep the VCO locked in phase and frequency to the data. The PLL acts like a flywheel, keeping a stable, regular bit clock that is largely immune to jitter in the recovered signal that drives one of the phase comparator inputs. The output of the VCO is the recovered bit clock.

Data recovery

The two '1's threshold outputs from the receiver are xor’ed together and then integrated. This is to minimize the effects of noise by summing the data over the whole bit period. Just before the end of the middle of the bit period, the integrator output is sampled at a time determined by the recovered bit clock. This squared sampled data stream is the final recovered serial data.

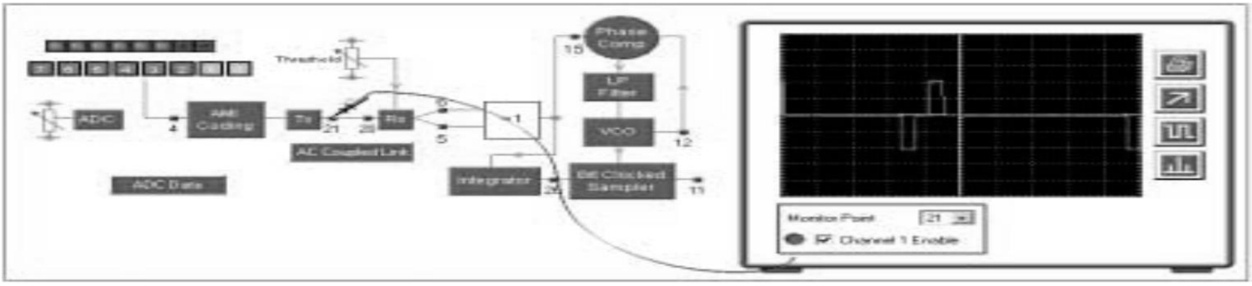
Problems associated with AMI

The AMI data format is very good however:

- For long streams of '0's, there are no level transitions in the data. This means that the pll will receive no control signal for long periods and may drift out of lock, resulting in corruption of data.

Procedure:

Set all controls to mid position. Select user data word or adc data using the button and adjust ***dc (5)*** control to create a serial data word. Observe this at monitor point ***4*** . Select an ac or dc coupled link. Observe the coded data word before and after the link monitor points ***21*** & ***20***. Note the signal offset for different data patterns for ac at monitor point ***2***



Monitor Point 21

☑ Channel 1 Enable

Figure 5.4

View the data at monitor point ***5***. Adjust the ***receiver threshold (8)*** control for a stable signal. View the signals in the bit clock recovery circuit at monitor points ***15*** & ***12***; adjust the ***synchronous bit clock (9)*** control for pll lock. Examine the signals in the data recovery path at monitor points ***26*** & ***11***. Answer the questions provided. You will need to make some observations in order to answer them.

Observations and results:

1. Are there any problems when an ac link is introduced?
2. Are there any problems for ***data words*** of:
   a. 11111111?
   b. 00000000?
   c. 10101010?

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Observation's Use ***Displays*** skills to use the observations from lab work for experimental verifications and illustrations.	Not able to use the observations from lab work for experimental verifications and illustrations.	Slightly able to use the observations from lab work for experimental verifications and illustrations.	Somewhat able to use the observations from lab work for experimental verifications and illustrations.	Moderately able to use the observations from lab work for experimental verifications and illustrations.	Fully able to use the observations from lab work for experimental verifications and illustrations.
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Equipment Handling ***Equipment care*** during the use.	Doesn't handle equipment with required care.	Rarely handles equipment with required care.	Occasionally handles equipment with required care.	Often handles equipment with required care.	Handles equipment with required care.
Group Work ***Contributes*** in a group based lab work.	Doesn't participate and contribute.	Slightly participates and contributes.	Somewhat participates and contributes.	Moderately participates and contributes.	Fully participates and contributes.

Weighted CLO (Psychomotor Score)	
Remarks	
Instructor's Signature with Date:	

LAB SESSION 06

Synchronization

Objective:

- To demonstrate word synchronization in digital data transmission

Equipment required:

Digital Data Formatting workboard 53-150 that comprises of following blocks:

- Signal generator
- Compressor
- Filter
- Pam generator
- Sample and hold circuit
- Analogue to digital converter
- Nrz, rz, bprz, sp, ami links
- Synchronization circuits
- Digital to analogue converter
- Expander

Theory:

In a recovered serial data stream, it is necessary to be able to find out where the start and end of each data word is.

This is done by including pre-defined synchronization words in the data stream.

When the receiver recognizes the specified sequence in the data, it produces a pulse.

The recovered bit clock is divided by the known word size to generate a word clock. This may not be word synchronized correctly however.

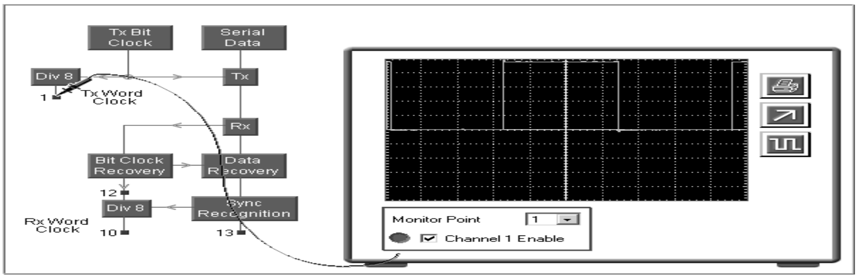
To correctly align the word clock, the counter that is used to divide the bit clock is reset by the pulse generated by the sync word recognizer.

There is a possibility that the sync word will accidentally be found in the data. This possibility can be reduced by lengthening the sync word.

Another way of reducing false syncs is for the receiver to know how often a sync word is being inserted in the data stream, and only look for syncs at specific, regular intervals.

Procedure:

Examine the Tx word clock at monitor point ***1***.



Monitor Point 1

● ☑ Channel 1 Enable

Figure 6.1

Observe the sync recognition pulses at monitor point ***13*** , the received bit clock at monitor point ***12*** , and the word clock that is derived from them at monitor point ***10*** . Adjust the ***Receiver threshold (8)*** control if necessary to get a stable display

<u>Observation and results</u>

a) What might happen if the sync word was 10101010?

b) Can the word clock synchronize falsely to patterns in the data that match, but are not, the real sync word?

c) Can the recovered sync word be useful for any other purpose than word synchronization?

d) How can the presence of a sync word assist in bit clock recovery? (Hint - what happens for data that is all '1's or all '0's?)

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Equipment Handling ***Equipment care*** during the use.	Doesn't handle equipment with required care.	Rarely handles equipment with required care.	Occasionally handles equipment with required care.	Often handles equipment with required care.	Handles equipment with required care.
Group Work ***Contributes*** in a group based lab work.	Doesn't participate and contribute.	Slightly participates and contributes.	Somewhat participates and contributes.	Moderately participates and contributes.	Fully participates and contributes.

Weighted CLO (Psychomotor Score)	
Remarks	
Instructor's Signature with Date:	

LAB SESSION 07

Amplitude shift keying

Objective:

- To demonstrate amplitude shift keying (ASK) modulation and demodulation.

Equipment required:

Modulation and Keying Workboard 53-160 which comprises the following blocks:

- Data Generator
- ASK, FSK, PSK, QPSK, DPSK, DQPSK Links

Theory:

Amplitude shift keying –ASK

In a digital communications system the modulating waveform will be in the form of a square wave, or pulse train. Ask is a form of amplitude modulation where the carrier is modulated by the pulse train.

In this form of modulation the sine carrier takes 2 amplitude values, determined by the binary data signal. In its simplest form the carrier is 'keyed', that is switched on and off for set periods to conform with the bit pattern of the modulating signal. Usually the modulator transmits the carrier when the data bit is “1”. It completely removes when the bit is”0”. This is known as on-off ask, or on-off keying (OOK). There are also ask shapes called multi-level where the amplitude of the modulated signal takes more than 2 values.

If the modulating waveform is not a sinusoid but is a square wave, or a pulse train, using on-off keying the equation becomes: $v(t) = a\cos \omega ct$ during the on period and $= 0$ elsewhere.

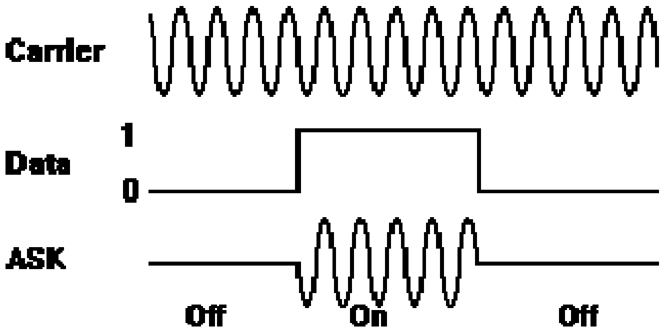

Figure 7.1: message signal (above) and corresponding ask signal (below)

The demodulation can be coherent or non-coherent. In the first case, more complex as concern the circuit but more effective as against the noise effect, a product demodulator multiplies the ask signal by the locally generated carrier. In the second case the envelope of the ask signal is detected via diode. In both cases the detector is followed by a low pass filter which removes the residual carrier component and a threshold circuit which squares the data signal.

Procedure:

Modulation

The system below shows a carrier being amplitude shift keyed by digital data which is set by the two rotary switches positioned to the centre-right of the workboard. Set all of the potentiometer controls to their mid positions. Set the MS bits switch (7) to 0 and the LS bits switch (8) to 1. Drag the probe to the available monitor points to observe the signals around the circuit using the oscilloscope.

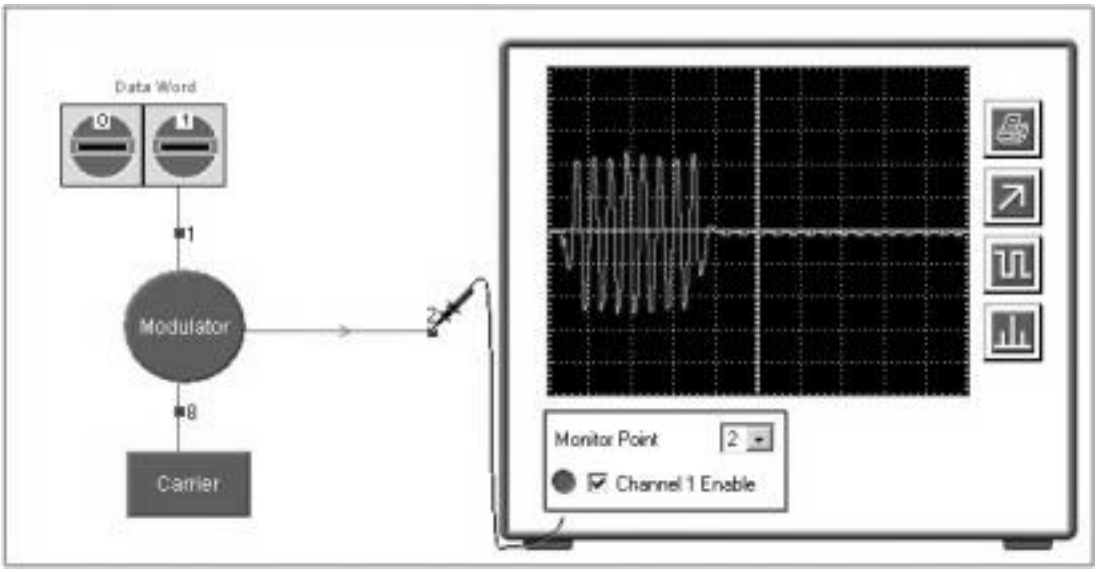

Figure 7.2 ASK Modulation

De-modulation

A diode detector has now been added to the Production of ASK practical. Set all of the potentiometer controls to their mid positions. Set the MS bits switch (7) to 0 and the LS bits switch (8) to 1. Drag the probe to the available monitor points to observe the signals around the circuit using the oscilloscope.

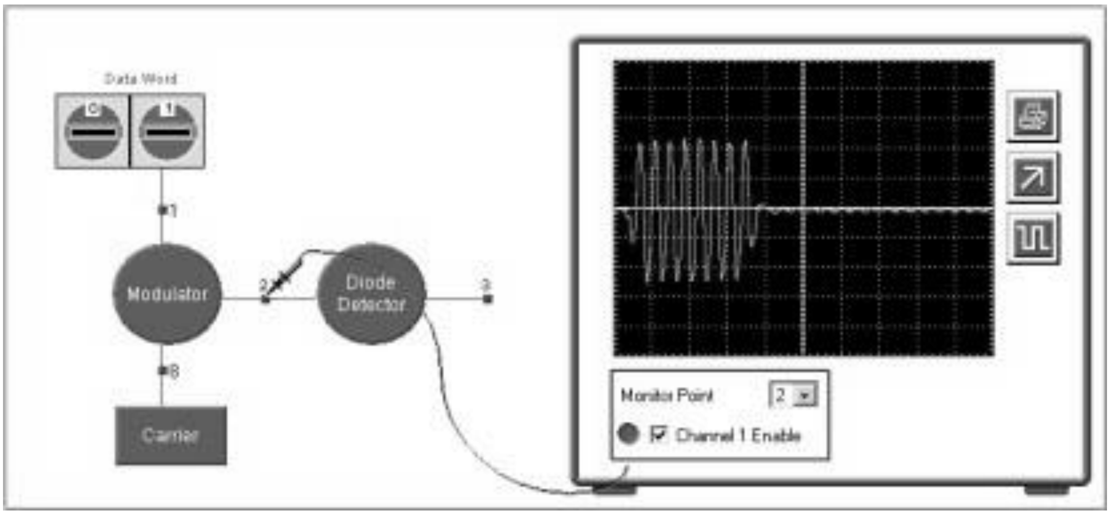

Figure 7.3 ASK Demodulation

Observation and Results

a) Make observations at different data pattern and observe the modulator and demodulator output
b) Why ripples are appearing at the output?

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Weighted CLO (Psychomotor Score)	
Remarks	
Instructor's Signature with Date:	

LAB SESSION 08

Binary Frequency Shift Keying

Objective:

- To demonstrate frequency shift keying (fsk) modulation and demodulation.

.

Equipment required:

Modulation and Keying Workboard 53-160 which comprises the following blocks:

- Data Generator
- ASK, FSK, PSK, QPSK, DPSK, DQPSK Links

Theory:

Frequency shift keying –FSK

In this modulation the sine carrier takes 2 frequency values, determined by the binary data signal. The modulator can be carried out in different ways:

- A voltage controlled oscillator (vco): a single voltage-controlled oscillator may be used with its frequency altered by the modulating signal voltage.
- A system transmitting one of the 2 frequencies as function of the data signal: the two frequencies may be produced by two oscillators and their outputs switched by the modulating signal.
- A frequency divider controlled by the data signal.

The most used demodulation techniques are the one using a pll circuit. The fsk signal across the pll input takes two frequency values. The error voltages supplied by the phase comparator follows such variations, and so, it constitutes the nrz binary representation (high and low level) of the fsk input signal. The pll demodulator is followed by a low pass filter, which removes the residual carrier components and a squarer circuit which forms the proper data signal.

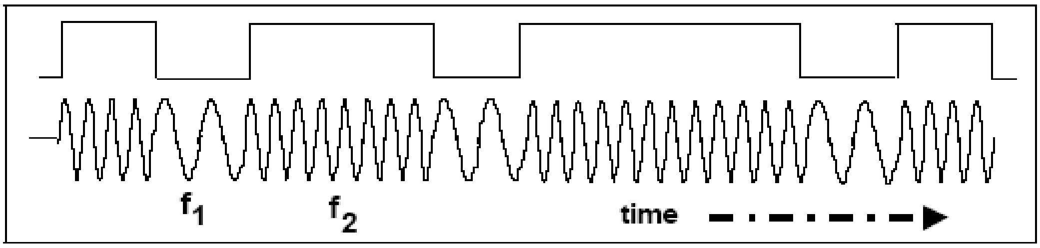

Figure 8.1: frequency shift keying

In our setup we have used a voltage controlled oscillator which switches its frequency with respect to the two states of binary signal.

Procedure:

Modulation

The system below is similar to that in the Amplitude Shift Keying Assignment except that a frequency modulator is being used rather than an amplitude modulator. Set all of the potentiometer controls to their mid positions. Set the MS bits switch (7) to 0 and the LS bits switch (8) to 1. Observe the signals around the circuit using the oscilloscope.

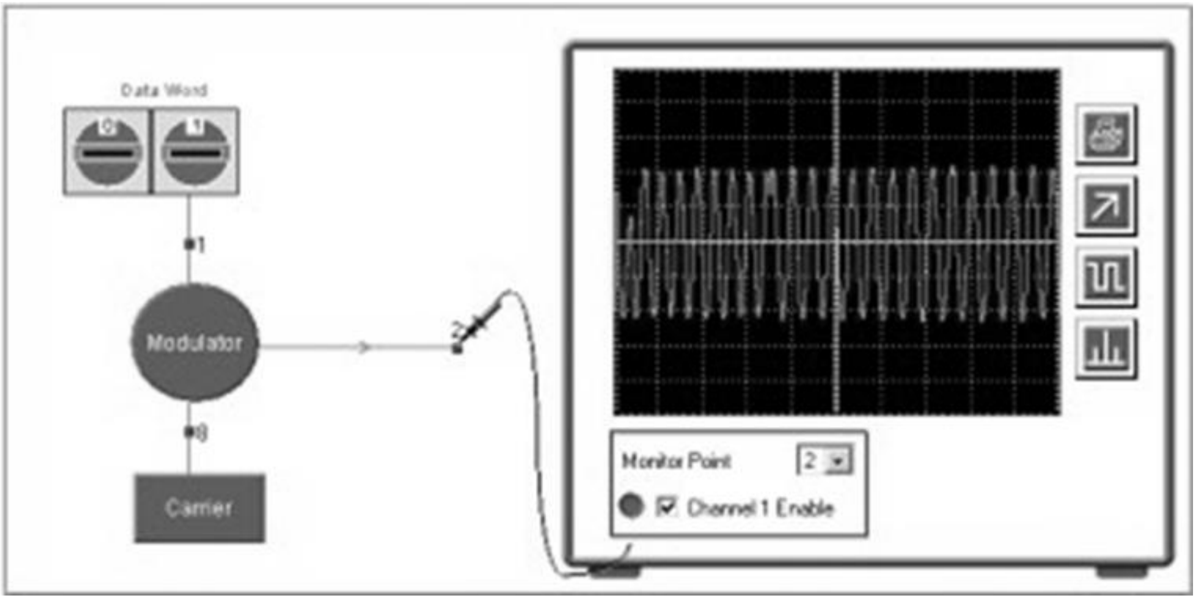

Figure 8.2 FSK Modulation

Demodulation

The system below shows a VCO and Phase Locked Loop detector for the demodulation of FSK. Set all the potentiometer controls to their mid positions. Set the MS bits switch (7) to 0 and the LS bits switch (8) to 0. Observe the signals around the circuit using the oscilloscope.

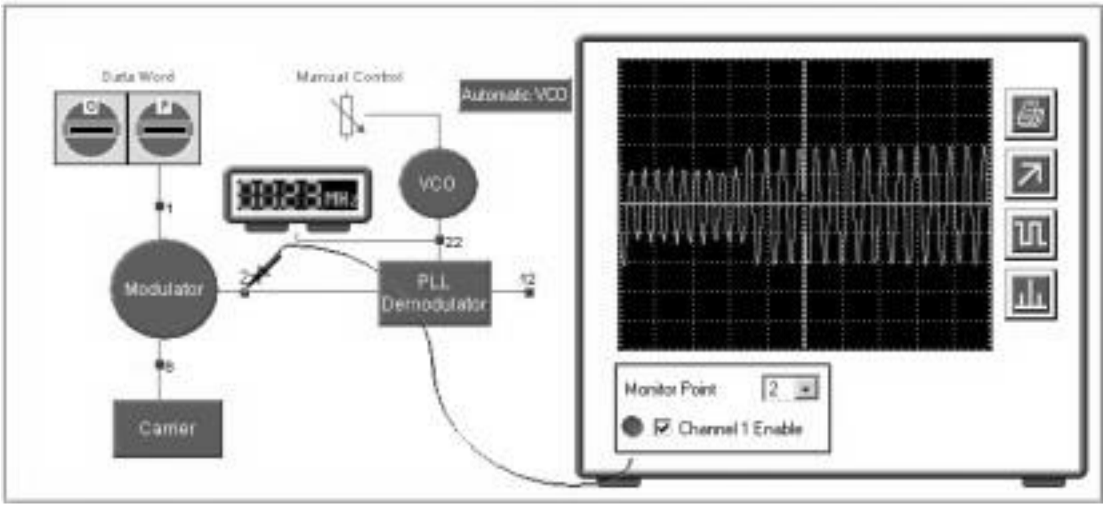

Figure 8.3 FSK Demodulation

Observation and Results

Make changes in data pattern and observe the output of the modulator and demodulators

Report your results below:

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Weighted CLO (Psychomotor Score)	
Remarks	
Instructor's Signature with Date:	

LAB SESSION 09

Binary Phase Shift Keying

Objective:

To demonstrate the 2 PSK (phase shift keying) modulation and demodulation.

Equipment required:

Modulation and Keying Workboard 53-160 which comprises the following blocks:

Data Generator
ASK, FSK, PSK, QPSK, DPSK, DQPSK Links

Theory:

Phase shift keying -PSK

In this kind of modulation the sine carrier takes 2 or more phase values, directly determined by the binary data signal (2-phase modulation) or by the combination of certain number of bits of the same data signal (n-phase modulation) 2 phase psk modulation is also called 2 PSK or binary PSK (BPSK) or phase reversal keying (prk). The sine carrier takes 2 phase valued determined by the binary data signal, modulation techniques is the one using a balanced modulator is the direct or inverted input carrier as function of the data signal.

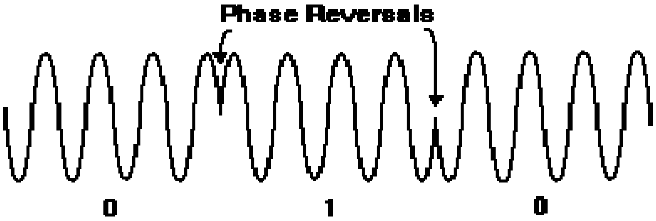


Figure 9.1 a PSK waveform

2PSK modulator

There are a number of methods of producing a PSK waveform.

One common method when phase shifts of plus and minus 90 degrees are used is shown in block diagram form below:

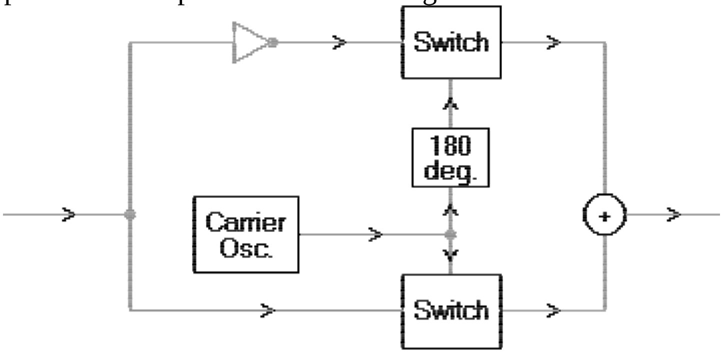


Figure 9.2 PSK Modulator

The phase shift does not have to be 180 degrees, although this is often used in practice as it allows the maximum separation of the digital states.

The switches can be implemented with numerous types of devices and circuits.

Two of the most popular types of circuit which are useful over a wide frequency range (up to 4 GHz, or so) are the balanced modulator using Schottky or hot carrier diodes, or dual- gate FET switches.

At relatively low frequencies, PSK may be produced digitally, rather than using balanced modulators.

This is done by using a shift register and clocking it from a carrier oscillator.

If taps are taken at various points down the shift register then different phases are produced. A switch can be used to select the two required phases for 1 and 0 states.

If the clocking oscillator is made variable, the phase shift can be made variable also.

2psk demodulator:

The demodulation is carried out using a phase locked loop demodulator as shown in procedure below:

Procedure:

Modulation

In this assignment the carrier is being phase modulated by the data waveform. Set all of the potentiometer controls to their mid positions. Set the ***MS bits switch (7)*** to 0 and the ***LS bits switch (8)*** to 1. Observe the signals around the circuit using the large oscilloscope display.

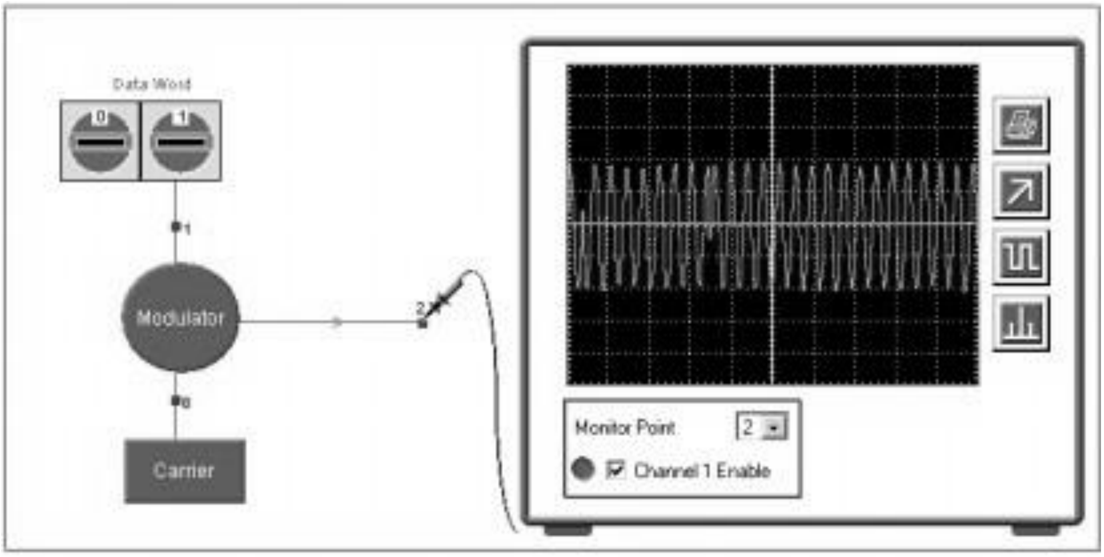
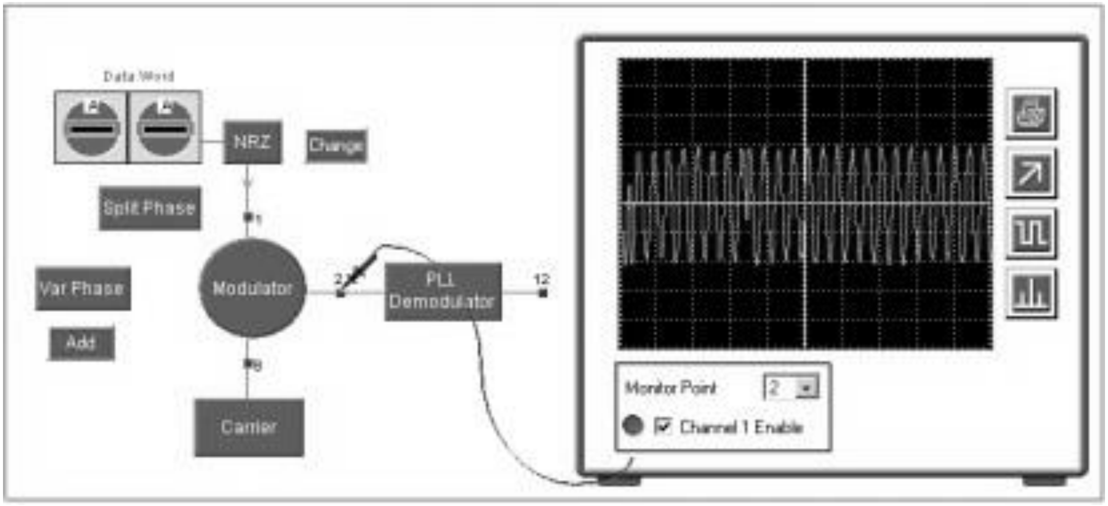


Figure 9.3 PSK Modulation

Demodulation

The carrier is being phase modulated by the data waveform. The phase shift of the PSK is +/-90 degrees, but can also be varied. Set all of the potentiometer controls to their mid positions. Set the ***MS bits switch (7)*** to A and the ***LS bits switch (8)*** to A. Observe the signals around the circuit using the oscilloscope.



Monitor Point 2

☑ Channel 1 Enable

Figure 9.4 PSK Demodulation

Observation and Results:

Make changes in data word and record your readings .Also change the phase control (4) and observe the changes in modulated output and demodulated output

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Weighted CLO (Psychomotor Score)	
Remarks	
Instructor's Signature with Date:	

LAB SESSION 10

The Costas Loop Demodulator

Objective:

Demonstration of costas loop for coherent detection at the receiver.

Equipment required:

Modulation and keying workboard 53-160 which comprises the following blocks:

- Data generator
- Ask, fsk, psk, qpsk, dpsk, dqpsk link

Theory:

Demodulation of psk using a costas loop

The costas loop provides an alternative way of demodulating psk transmissions. It uses a phase locked loop to produce a carrier frequency reference of constant phase which is then multiplied by the incoming psk signal to produce a demodulated data output.

The block diagram below shows the three multipliers (modulators) and the vco which form the costas loop.

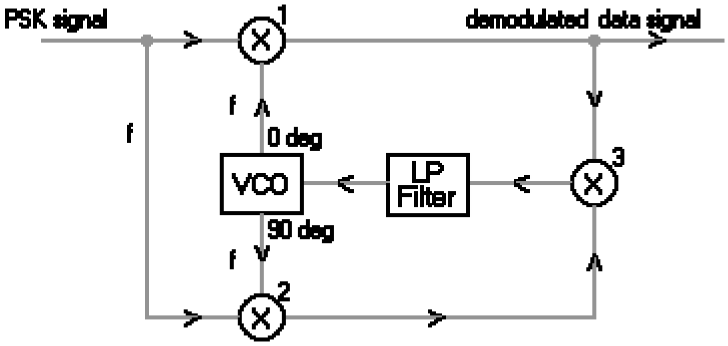

Figure 10.1 costas loop

If the vco is locked to the incoming carrier then:

$$\Omega_{vco} = \omega_c$$

Only a small phase difference, $ø_e$ will be present.

Let the two outputs from the vco be: 2cos ω_ct in phase with the carrier 2sin ω_ct in quadrature.

The psk signal input is:

$$S(t) = a \cos [\omega_c t + ø]$$

Where ø is 0 or π depending on whether the state of the digital input d is 1, or -1.

So, if d(t) is the state of the digital input, this signal expression can be written:

$$S(t) = a\, d(t) \cos \omega_c t$$

The multiplier outputs are the products of the two inputs to each. Thus these outputs are:

$$[a\, d(t) \cos \omega_c t][2\cos \omega_c t] \text{ and}$$

$$[a\, d(t) \cos \omega_c t][2\sin \omega_c t] .$$

The reference channel output is used; i.e.,

$$V_{out} = [a\, d(t) \cos \omega_c t][2\cos \omega_c t]$$

$$= 2a\, d(t) \cos 2\, \omega_c t$$

Now, $\cos 2x = 0.5[1 + \cos 2x]$, so the expression for v_{out} becomes:

$$V_{out} = 2a\, d(t)\, [0.5 + 0.5\cos 2\omega_c t]$$

$$= a\, d(t) + a\, d(t) \cos 2\omega_c t$$

This expression has two components: a dc component dependent on the phase of the digital input data and a component at twice the carrier frequency.

This double-frequency component can be removed by a post detection filter.

When the loop is in lock in figure 8.1, the vco will be phase-locked by modulators (2) and (3), causing it to produce an output from its f90 terminal that leads the incoming signal by 90 degrees. Since the vco produces outputs which differ by 90 degrees, the reference signal from the f0 output will be in phase with the incoming psk signal for, say, binary 1 and 180 degrees out of phase for binary 0.

The multiplying action of modulator (1) will then produce a positive dc level when the received and reference signals are in phase and a negative level when they are in anti-phase.
Subsequent data recovery circuits convert the bipolar output from the costas loop demodulator to unipolar nrz data.
It should be noted that when the incoming signal changes state, the sign of both inputs to modulator (3) change simultaneously so that its output remains constant and the VCO will be locked in at constant phase. If there is no information which specifies which of its phase values is +90 degrees and which is -90 degrees with respect to the reference, the demodulated data could be inverted (binary 1 and binary 0 interchanged).

This is a difficulty that cannot be resolved unless we know more about the signal than just that it is +/-90 degrees PSK. This ambiguity can be resolved by extending the use of a sync word pattern which is
Transmitted at regular intervals.

The pattern is chosen, not only to provide synchronization information, but to provide a bit sequence that can be identified as either correct, or inverted. When an inverted bit pattern is detected the logic circuits in the receiver re-invert the data to restore the correct sense.

Procedure:

- Connect the modulation and keying work board.
- Power the module. The carrier is being phase modulated by the data waveform. The phase shift of the psk is +/-90 degrees, but can also be varied
- Set all the potentiometer controls to their mid position.
- Set the **ms bits switch (7)** to a and the **ls bits switch (8)** to a.
- Observe the signals around the circuit using the oscilloscope.

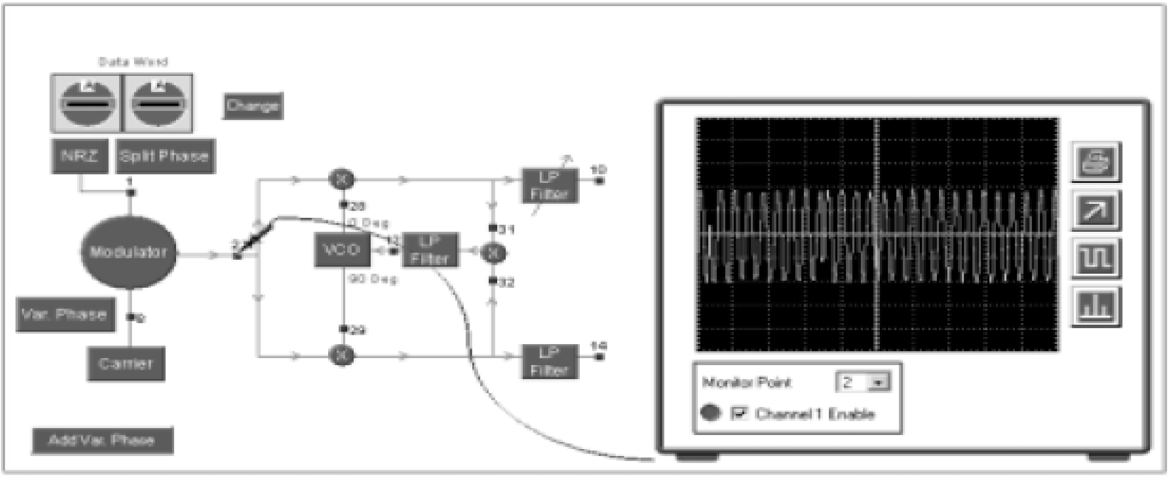

Figure 10.2

Observations & results:

1. Do the waveforms at monitor point 1 correspond with the formats selected?
2. Do the waveforms at monitor point 2 show psk?
3. Select nrz format and ensure that var. Phase is not selected. Is the required demodulated output present at monitor point 10?
4. Look at monitor point 31.
   a. Is the required demodulated output present at this monitor point?
   b. What needs to be done to provide the required output?
5. Go to monitor point 10 again and vary the pdf control (9). What effect does this have on the demodulated output?
6. Look at the vco control voltage at monitor point 12. How does this vary in response to the incoming psk? (you can decrease the selectivity of the lp filter by turning the pll filter control (6) towards minimum to see the effect better).
7. Set both the ms bits switch (7) and the ls bits switch (8) to 0. Does the demodulator output correspond to the data input?
8. Set both of the data switches to 1.
   a. Does the output correspond now?
   b. What can you say about the costas loop demodulator compared with the PLL demodulator as regards to nrz formatted data demodulation?
9. Repeat above procedure with split phase format(manchester)?

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Weighted CLO (Psychomotor Score)	
Remarks	
Instructor's Signature with Date:	

LAB SESSION 11

Quadrature Phase Shift Keying

Objective:

To demonstrate QPSK modulation & demodulation.

Equipment required:

Modulation and keying workboard 53-160 which comprises the following blocks:

- Data generator
- ASK, FSK, PSK, QPSK, DPSK, DQPSK link

Theory:

Modulation of QPSK

Quadrature phase shift keying (QPSK) in an extension of the simple PSK method of keying investigated in the phase shift keying assignment.

In QPSK the signal can take up one of four possible phase angles, mutually in quadrature, each corresponding to a particular data input condition.

Consider NRZ formatted data in which each word is divided into bit pairs instead of individual bits.

There are four possible ways of pairing binary 1 and 0. These are:

00
01
10
11

Any data word with an even number of bits may be represented by a combination of these bit pairs. One of the four phase angles is assigned to each of these bit pairs.

QPSK offers twice as many data bits per carrier phase change than binary phase shift keying (BPSK), and hence finds wide application in high-speed carrier-modulated data transmission systems.

For example, if the data transfer rate is 9600 bits per second the transmission line signaling rate will have 4800 bit pairs per second and thus will be at 4800 baud.

Typically, the four phases chosen foe QPSK are +/-45 degrees and +/-135 degrees. Each of these is assigned a bit pair (dibit).

The diagram shows a possible dibit pattern, often referred to as a constellation because of its star shape.

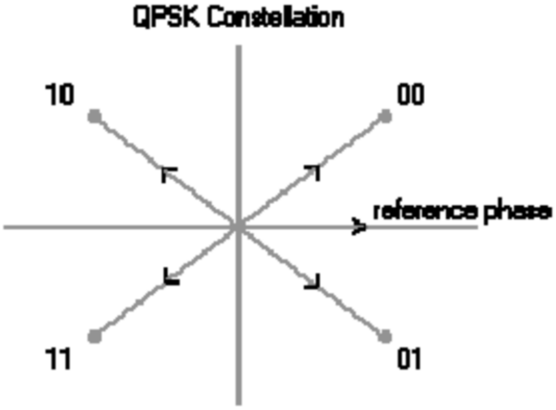


Figure 11.1 QPSK constellation diagram

In practice, the generation of the bit pairs may be done in a number of different ways. The simplest method is to store two bits, read off the combination and generate the required carrier phase shift and then store the next two bits, etc. A block diagram of such a system is shown below:

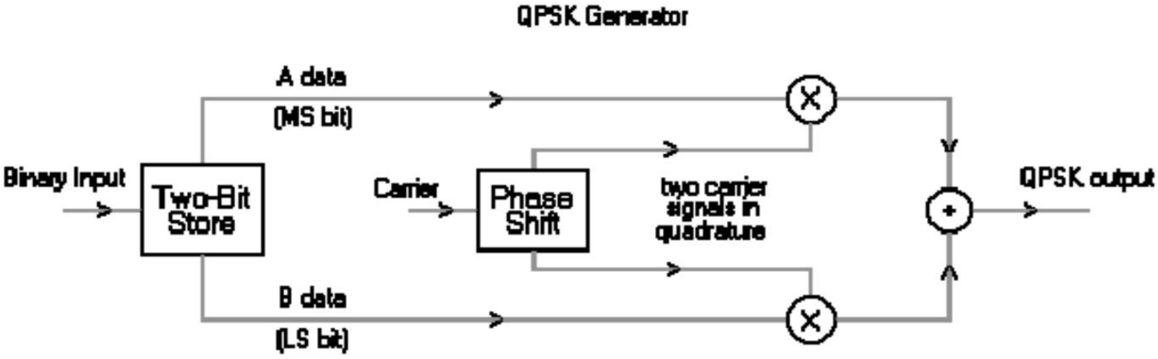


Figure 11.2

The expression for this QPSK will then be:

$$S(t) = \cos(\omega ct + \varphi)$$

Where:

$\Phi = +\pi/4, -\pi/4, +3\pi/4, -3\pi/4.$

By trigonometric expansion, this can be written:

$$S(t) = a\cos\omega ct + b\sin\omega ct$$

Where a and b are given values corresponding to the four possible angles.

For the angles chosen, these will be:

$(2a^{1/2}, 2b^{1/2}) = (1, 1), (-1, 1), (-1, -1), (1, -1)$

The transmitted signal is therefore the sum of two waveforms in quadrature.

Demodulation of QPSK

The received QPSK signal must be demodulated to produce the two components of the single transmitted. This is to combat the problems of phase ambiguity (these have already been met in the assignment for psk).

A phase detector is a mixer, whose action is one of multiplication. In a phase detector the two signals to be multiplied have the same frequency, thus the output of the detector will contain sum and difference frequency components. The sum component will be at double the carrier frequency and the difference component will be at dc.

That is, if the inputs to the detector are $\cos(\omega ct + \varphi)$ and $\cos \omega ct$ the output will be:

$$\cos(\omega ct + \varphi) \times \cos \omega ct = 0.5 \cos[(\omega ct + \varphi) + \omega ct] + 0.5 \cos[(\omega ct + \varphi) - \omega ct]$$

$$= 0.5 \cos 2(\omega ct + \varphi) + 0.5 \cos \varphi$$

Where φ is the transmitted data phase.

A low-pass filter is used to attenuate the second harmonic (double frequency) term, leaving:

$$V_o = 0.5 \cos \varphi$$

Φ is the modulated phase shift (+/-$\pi/4$, +/-3 $\pi/4$) and vo is the output dc voltage representing the appropriate dibit.

Now 0.5 cos (+/-45 degrees) = +0.35, and therefore the detector does not know if +45 degrees, or -45 degrees was sent.

Similarly, 0.5 cos (+/-135 degrees) =-0.35, and the same ambiguity exists.

In order to resolve these ambiguities, a second detector operating in quadrature is required. This can be achieved from the double costas loop type circuit, as shown below

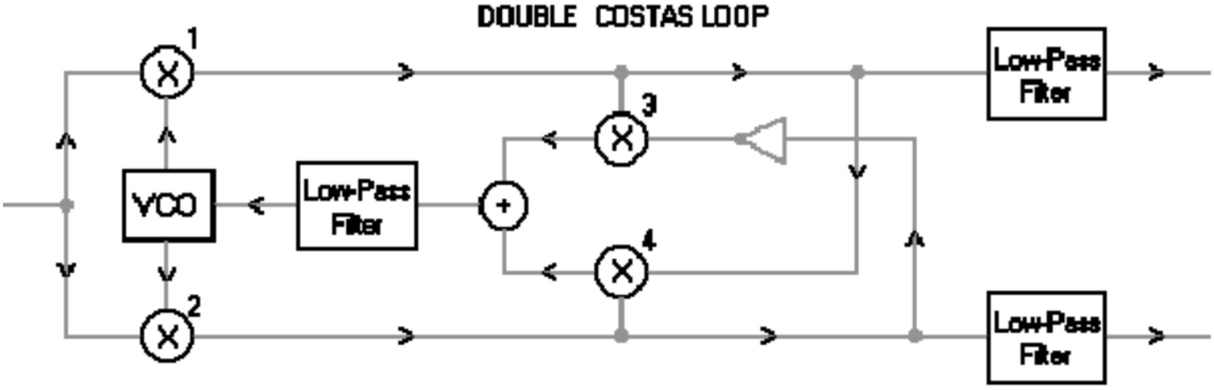


Figure 11.3

The inputs to the second detector are $\cos(\omega ct + \varphi)$ and $\sin \omega ct$ and the output will be:

$$\cos(\omega ct + \varphi) \times \sin \omega ct = 0.5 \sin[(\omega ct + \varphi) + \omega ct] + 0.5 \sin[(\omega ct + \varphi) - \omega ct]$$

$$= 0.5 \sin(2\omega ct + \varphi) - 0.5 \sin \varphi$$

Where φ is the transmitted data phase.

Again, a low-pass filter iss used to attenuate the second harmonic (double frequency) term, leaving:

$$V_o = 0.5 \sin \varphi$$

Φ is the modulated phase shift (+/- $\pi/4$, +/– 3 $\pi/4$) and vo is the output dc voltage representing the appropriate dibit.

The outputs of the two modulators are multiplied together to produce the vco control signal, giving:

$$0.5[\cos(2\omega ct + \varphi) + \cos \varphi] \times 0.5[\sin(\omega ct + .\,\Phi) - \sin \varphi]$$

$$= 0.25[\cos(2\omega ct + \varphi)][\sin(2\omega ct + \varphi)] - [\cos(2\omega ct + \varphi)][\sin \varphi] + [\sin(2\omega ct + \varphi)][\cos \varphi] - [\cos \varphi][\sin \varphi]$$

Expanding these terms, using the identity:

$$\cos a . \sin b = 0.5[\sin(a + b) - \sin(a - b)]$$

$$= 0.25[0.5 \sin 2(2\omega ct + \varphi) - 0.5[\sin(2\omega ct + \varphi) - \sin 2\omega ct] + 0.5[\sin(2\omega ct + 2\varphi) - \sin 2\omega ct] - 0.5 \sin 2\varphi]$$

Which simplifies to:

$= 0.125\ [0.5 \sin 2(2\omega ct + \varphi) - 0.5 \sin 2\varphi$

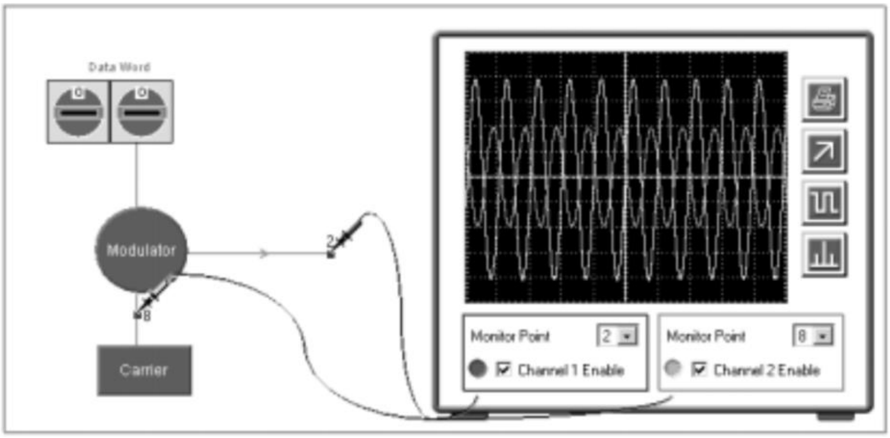
$= 0.125\ [\sin (4\omega ct + \varphi) - \sin 2\ \varphi]$

This contains a 4ωc term, which will be filtered out, leaving a dc term proportional to the phase shift which is used to control the vco.

Procedure:

Modulation

- Connect the modulation and keying work board.
- Power the module.
- Set all the potentiometer controls to their mid position.
- Set the **ms bits switch (7)** and the **ls bits switch (8)** to 0.
- Monitor the signal before modulation at monitor point 2.see figure 6.4



Monitor Point 2
● ☑ Channel 1 Enable

Monitor Point 8
● ☑ Channel 2 Enable

Figure 11.4

Observations & results:

- What are the four di-bits?

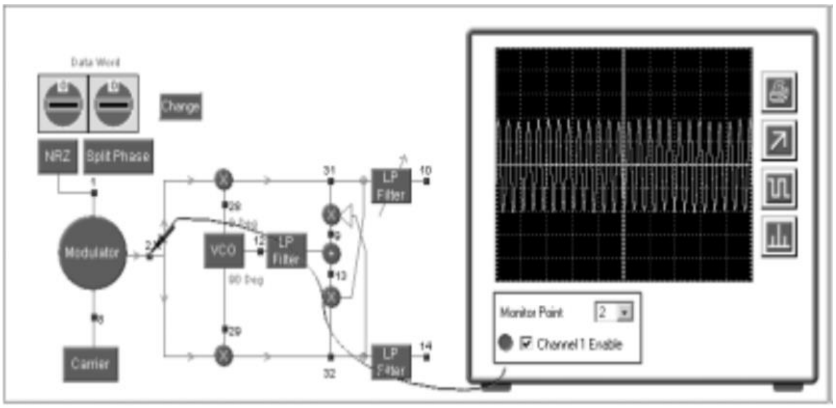
- Look at the monitor point 2 with the oscilloscope, the yellow trace is the carrier and the green trace is the modulated output.
  1. Are the two waveforms in phase?
  2. What is the phase shift of the output relative to the carrier?

- Repeat the above set of observations by:
  Setting the **ms bits switch (7)** and the **ls bits switch (8)** to f
  Setting the **ms bits switch (7)** to 0 and the **ls bits switch (8)** to f
  Setting the **ms bits switch (7)** to f and the **ls bits switch (8)** to 0

  1. Do the four possible combinations of dibits give the four phase shifts?
  2. Can you see the phase shifts in the output waveform?

Demodulation

- Set all the potentiometer controls to their mid position.
- Set the **ms bits switch (7)** and the **ls bits switch (8)** to 0.
- Observe the signal after demodulation at monitor points 10 & 14 using the oscilloscope. See figure 6.5



Monitor Point 2

☑ Channel 1 Enable

Figure 11.5

Observations & results:

- Set the **ms bits switch (7)** to 0 and the **ls bits switch (8)** to 5.
    1. what dibit pattern does this give?
    2. What QPSK output pattern do these settings give?

- Look at monitor point ***2*** with the large oscilloscope display. Can you see the 180 degree phase changes between the dibits?

- Look at the two outputs of the double costas loop (monitor pints ***10*** and ***14***).
    1. are the waveforms the same?
    2. Ignoring the small variations present on one of the outputs, do they correspond to the originating two data bit patterns?

- Monitor the output that corresponds to the ls bits pattern. Turn the carrier level control (5) to minimum and back to maximum a number of times and observe the output.
    1. Does the output always come up the same?
    2. Does it always correspond to the ls bits pattern?

- Turn the ***carrier level control (5)*** up and down until the output is in a state that does not correspond with the ***ls bits*** pattern. Look at the other output.
    1. Does this now correspond with the ls bits pattern?
    2. Is there ambiguity as to which output corresponds to which bit in each di bit? How can this be overcome in practice?

F/OBEM 01/05/00

NED University of Engineering & Technology
Department of Telecommunications Engineering
Course Code and Title: TC-311 Digital Communication and Information Theory

Laboratory Session No. _____________ Date: ______________________

Psychomotor Domain Assessment Rubric-Level P3					
Skill Sets	Extent of Achievement				
	0	1	2	3	4
Equipment Identification Sensory skill to ***identify*** equipment and/or its component for a lab work.	Not able to identify the equipment.	--	--	--	Able to identify equipment as well as its components.
Equipment Use Sensory skills to ***demonstrate*** the use of the equipment for the lab work.	Doesn't demonstrate the use of equipment.	Slightly demonstrates the use of equipment.	Somewhat demonstrates the use of equipment.	Moderately demon strates the use of equipment.	Fully demonstrates the use of equipment.
Procedural Skills ***Displays*** skills to act upon sequence of steps in lab work.	Not able to either learn or perform lab work procedure.	Able to slightly understand lab work procedure and perform lab work.	Able to somewhat understand lab work procedure and perform lab work.	Able to moderately understand lab work procedure and perform lab work.	Able to fully understand lab work procedure and perform lab work.
Response Ability to ***imitate*** the lab work on his/her own.	Not able to imitate the lab work.	Able to slightly imitate the lab work.	Able to somewhat imitate the lab work.	Able to moderately imitate the lab work.	Able to fully imitate the lab work.
Observation's Use ***Displays*** skills to use the observations from lab work for experimental verifications and illustrations.	Not able to use the observations from lab work for experimental verifications and illustrations.	Slightly able to use the observations from lab work for experimental verifications and illustrations.	Somewhat able to use the observations from lab work for experimental verifications and illustrations.	Moderately able to use the observations from lab work for experimental verifications and illustrations.	Fully able to use the observations from lab work for experimental verifications and illustrations.
Safety Adherence Adherence to ***safety*** procedures.	Doesn't adhere to safety procedures.	Slightly adheres to safety procedures.	Somewhat adheres to safety procedures.	Moderately adheres to safety procedures.	Fully adheres to safety procedures.
Equipment Handling ***Equipment care*** during the use.	Doesn't handle equipment with required care.	Rarely handles equipment with required care.	Occasionally handles equipment with required care.	Often handles equipment with required care.	Handles equipment with required care.
Group Work ***Contributes*** in a group based lab work.	Doesn't participate and contribute.	Slightly participates and contributes.	Somewhat participates and contributes.	Moderately participates and contributes.	Fully participates and contributes.

Weighted CLO (Psychomotor Score)	
Remarks	
Instructor's Signature with Date:	

LAB SESSION 12

Differential Phase Shift Keying

Objective:

To demonstrate DPSK modulation and demodulation.

Equipment required:

Modulation and keying workboard 53-160 which comprises the following blocks:

- Data generator
- Ask, fsk, psk, qpsk, dpsk, dqpsk links

Theory:

Modulation of dpsk

With simple psk there is a reference phase about which the phase of the transmitted wave shifts as it is modulated.

With this type of system, both the transmitter and the receiver have to maintain an absolute phase reference against which the received signal is compared.

With differential phase shift keying (dpsk) the data is transmitted in the form of discrete phase shifts, where the phase reference is the phase of the previously transmitted signal phase.

The advantage of this technique is that an absolute phase reference does not have to be maintained.

A simple way to produce dpsk is shown in the diagram below:

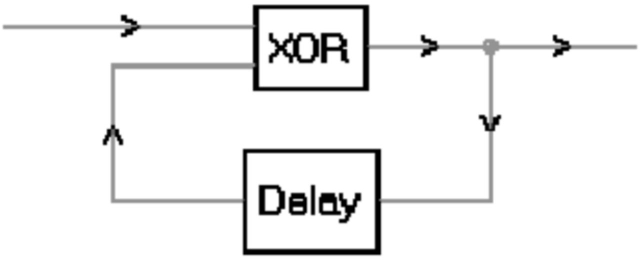


Figure 12.1

Consider the data word 10010110 and assume that the initial state of the delayed input to the exclusive-or gate is 0. The data word can be written:

1 0 0 1 0 1 1 0
Do d1 d2 d3 d4 d5 d6 d7

Taking the data word bit by bit gives:

Do excl-or 0 (the initial value of the delayed input) = 1
D1 excl-or 1 (the resulting value from above) = 1
D2 excl-or 1 = 1
D3 excl-or 1 = 0
D4 excl-or 0 = 0 ....etc
Giving a resulting output word from the excl-or gate of:

1 1 1 0 0 1 0 0

This word is now used to modulate a binary phase shift modulator.

Let the binary 0 state correspond to an output phase of 0 radians (0 degrees) and a binary 1 to a phase of π radians,(180 degrees) giving:
π π π 0 0 π 0 0
As the dspk output phase.

Demodulation of dpsk

The diagram below shows the form of a typical dpsk demodulator:

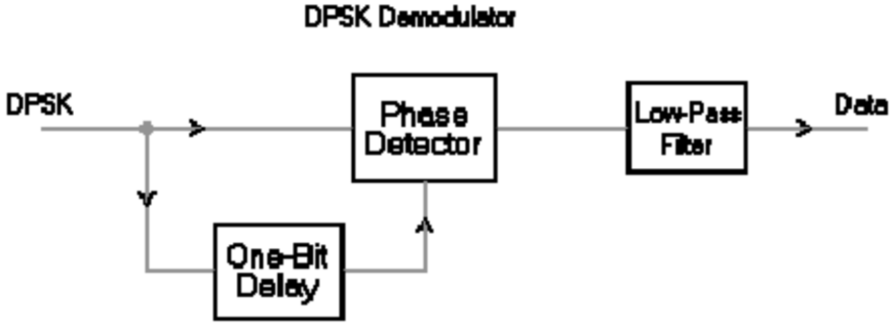


Figure 12.2

The inputs to the phase detector are the received signal and that signal delayed by one bit period.

The phase detector produces a negative output voltage when the input phases are the same and a positive voltage when they are in antiphase.

Thus, for the example of dpsk generation shown before, the inputs to the phase detector will be:

Direct input: π π π 0 0 π 0 0

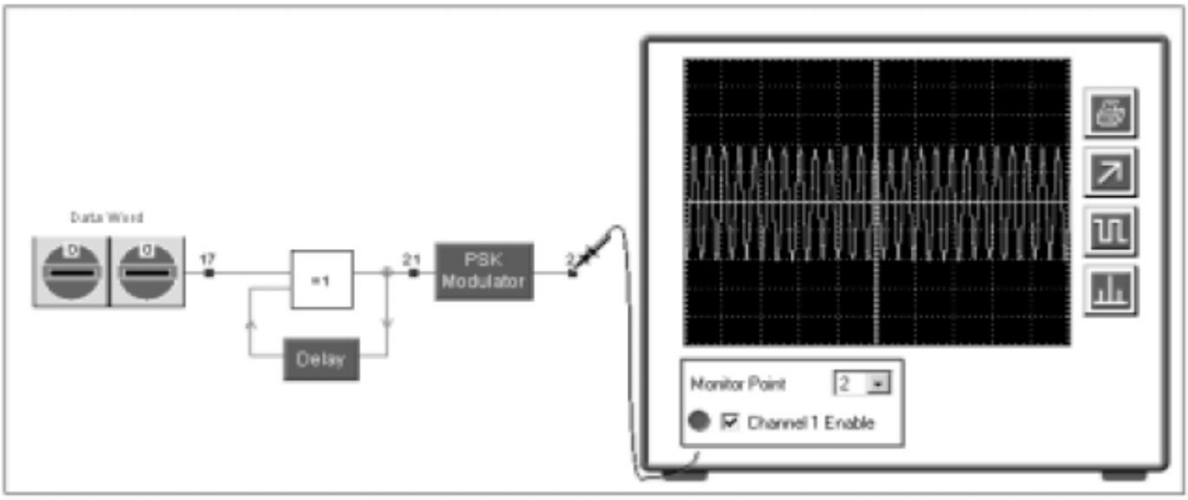
Delayed input: 0 π π π 0 0 π 0
giving an input of:
\- + + - + - - +
Which, when put through a comparator, gives:
1 0 0 1 0 1 1 0
Which is the original data word.

Procedure:

- Connect the modulation and keying work board.
- Power the module.

Modulation

- The data is applied to an exclusive-or gate and delay circuit to differentially pre-code it
- Before being applied to a phase modulator.
- Set all the potentiometer controls to their mid positions.
- Set the **ms bits switch (7)** and the **ls bits switch (8)** to 0.
- Monitor the signal before and after modulation at monitor points 17, 21 & 2 .see figure



Monitor Point 2

● ☑ Channel 1 Enable

Figure 12.3

Observations and results:

- Look at the monitor point 17 with the oscilloscope:
  1. Does the data input to the dpsk modulator changes with time?
  2. What binary data does this represent?

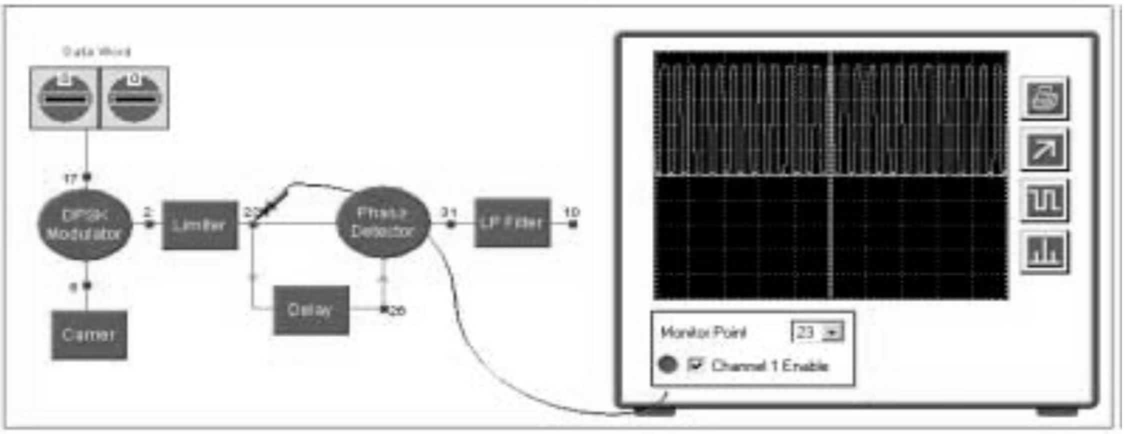
- Now look at monitor point 21 with the oscilloscope. Does the state of exclusive-or output changes with time?

- Now look at the monitor point 2 with the oscilloscope:
  1. Does the phase of modulated output changes with time?
  2. How is the phase of the modulated output related to the data input?

- Repeat these set of observations by setting the **ms bits switch (7)** and the **ls bits switch (8)** to f.

Demodulation

- Observe the signal after demodulation at monitor points 31 & 10 using the oscilloscope. See figure.



Monitor Point 23

● ☑ Channel 1 Enable

Figure 12.4

Observations and results:

Ensure that the **ms bits switch (7)** and the **ls bits switch (8)** to 0.

- Look at monitor point *2* with the large oscilloscope display. Does the dpsk waveform change phase as you would expect?
- Look at the output of phase detector, monitor point 31, with the oscilloscope. Does the waveform corresponds to the originating data?
- Try a number of the **ms bits switch (7)** and the **ls bits switch (8).** Do the waveforms corresponds to the originating data?

F/OBEM 01/05/00

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Course Code and Title: TC-311 Digital Communication and Information Theory
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Psychomotor Domain Assessment Rubric-Level P3					
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Weighted CLO (Psychomotor Score)	
Remarks	
Instructor's Signature with Date:	

LAB SESSION 13

Open Ended Lab

Problem Statement

Cameras are now a days provided with more and more megapixels for better image quality but this also increase the size of the image which results in delay of image transmission via internet because of poor internet speed. This generates the need for some data compression method to be applied on image or other data for fast transmission. There are many algorithm for data compression some are loss less some are lossy. Propose a data compression algorithm that can compress the image without degrading the quality significantly. Use some simulation software for implementation of your proposed algorithm

Instruction:

- Select image and algorithm as per your preference implement it using any simulation tool.
- This task can be performed in group of four
- Each member should contribute equally
- Calculate Mean Square error for your compressed image (should be as minimum as possible)
- Calculate Peak Signal to Noise Ratio for your compressed image
- Submit a report comprising of background knowledge of your selected algorithm, simulation code , calculations, result and contribution of each member

F/OBEM 01/18/00

NED University of Engineering & Technology
Department of Telecommunications Engineering
Course Code & Title: TC-311 Digital Communication and Information Theory
Assessment Rubric for CEP

Criterion	**Level of Attainment**				
	Below Average (0)	**Average (1)**	**Good (2)**	**Very Good (3)**	**Excellent (4)**
Timely submission	Not submitted on time				Submitted on time
Literature review for image compression techniques	No details provided	Only basic information given	Few pros and cons are discussed with some basic information	Detailed discussion on the techniques but methodology not discussed	All details are provided including pros , cons and methodology
Simulation and calculations	Unable to run simulation	Unsatisfactory results	Partially satisfactory results	Partially unsatisfactory results	Satisfactory results
Response to question	Unable to answer any question	Answered only basic questions	Answered few questions with in depth knowledge	Answered most of the technical questions	Answered all technical questions

Student’s Name: ___________________________ Roll No.: __________________________________

Total Score = ______________________________ Instructor’s Signature: _______________________